EE511 SYLLABUS

• Course Name: Computer Architecture
• Prerequisite: Logic design (EE203),
Introduction to computer architecture (EE312)
• Instructor: In-Cheol Park (icpark@kaist.edu, Tel. 042)350-3461, NanoFab Center 320)
• Teaching Assistant: 김대성, Daesung Kim (dskim@ics.kaist.ac.kr, Tel. 042) 351-9885)
• Homepage: http://ics.kaist.ac.kr/ee511_2018s.php

• Course Description

The goal of this course is to understand the principles and organization of computer systems, and to learn the performance enhancing techniques and quantitative analysis methods used in advanced processors. This course covers high-performance techniques such as pipelining and out-of-order processing, memory hierarchy including cache memory and virtual memory, interrupt processing, and how to design a processor based on quantitative analysis. In addition, recent important topics such as SIMD and multiprocessors will be introduced, and a design and simulation for a simple processor is to be practiced in order to enhance the comprehensive understanding of computer systems.

• Main Textbook

J. Hennessy and D. Patterson, "Computer Architecture: A Quantitative Approach", Morgan Kaufmann Publishers Inc.

• Term Projects

Two design projects will be conducted to gain practical design experiences on a simple processor. We first develop a software simulator for the processor, and then design it in Verilog HDL based on a pipelined architecture.

• Tentative Timetable

Week	Main Contents	Reference
1	Review of Computer History	
2	Review of Undergraduate Computer Architecture	
3	Verilog HDL	
4	Verilog HDL	
5	Quantitative Performance Analysis & Instruction set principles	
6	Advanced Pipelining	
7	Multiple issue & Dynamic Scheduling	
8	Mid-Term Exam.	
9	Branch prediction	
10	Computer Arithmetic & Datapath design	
11	Controller design	
12	Interrupt Processing	
13	Cache memory	
14	Virtual memory	
15	Interconnection networks	
16	Final Exam.	