

Fast Frequency Acquisition All-Digital PLL Using PVT Calibration

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Abstract—Fast frequency acquisition is crucial for phase-locked loops (PLLs) used in portable devices, as on-chip clocks are frequently scaled down or up in order to manage power consumption. This paper describes a new frequency acquisition method that is effective in all-digital PLLs (ADPLLs). To achieve fast frequency acquisition, the codeword of the digitally controlled oscillator (DCO) is predicted by measuring the variations of process, supply voltage and temperature (PVT). A PVT sensor implemented with a ring oscillator is employed to monitor the variations. As the sensor frequency at the current operating condition is directly related to the PVT variations, the sensor frequency is taken into account to compensate such variations in predicting the DCO codeword. The proposed method enables one-cycle frequency acquisition, and the frequency error is less than 1.5%. The proposed ADPLL implemented in a 0.18 μm CMOS process operates from 150MHz to 500MHz and occupies 0.075mm².

I. INTRODUCTION

The all-digital phase-locked loop (ADPLL) has been intensively researched for clock generation [1][2], and clock data recovery [3], and recently its application area is expended to frequency synthesis [4]. The role of the ADPLL is almost similar to that of the charge-pump phase-locked loop (CPPLL), that is, generating an output clock frequency that is a (integer or fractional) multiple of the given reference input clock. The difference between the CPPLL and the ADPLL is the way of controlling oscillators. The digital codeword is used to control the oscillation frequency in the ADPLL, whereas the analog voltage in the CPPLL.

The ADPLL has many advantages over the classical CPPLL. First, the ADPLL is immune to the digital switching noise generated in a VLSI system, as the digital codeword is more tolerable against noise and can more accurately express the control information than the voltage signal [1]. Second, the ADPLL can have a fast design turnaround time, because it can be implemented using automated CAD tools instead of relying on the full-custom design [4]. Third, actually most important, frequency acquisition is fast in the ADPLL.

The process of bringing the loop into lock is called acquisition [5]. The acquisition can be divided into frequency acquisition and phase acquisition. The primary advantage of the ADPLL is that the acquisition is fast, as induced from its digital nature [1]. In portable devices, fast frequency acquisition is essential to manage power by employing the dynamic frequency scaling (DFS) technique [6]. During the last decade, lots of techniques have been presented for fast

acquisition. An ADPLL associated with 7-cycle acquisition was proposed in [7]. The time-to-digital converter (TDC) matched with the resolution of the digitally controlled oscillator (DCO) was used in [7] to achieve fast acquisition, but its output frequency was low (< 60MHz). In [8], an ADPLL that can achieve frequency acquisition in 2 cycles was proposed by employing two DCOs, but it suffers from the large area overhead resulting from the duplicated DCOs.

This paper presents a new ADPLL associated with the method for fast frequency acquisition. To achieve fast frequency acquisition, the DCO codeword is predicted by measuring the variations of process, supply voltage and temperature (PVT). A ring oscillator called a PVT sensor is employed to monitor the variations. By taking into account the sensor frequency to compensate such variations in predicting the DCO codeword, the proposed method enables one-cycle frequency acquisition.

II. PROPOSED PREDICTION OF THE DCO CODEWORD

To achieve fast frequency acquisition, the DCO codeword should be predicted for the desired output frequency. Assuming that DCO output period is linearly proportional to the DCO codeword, we can easily predict the DCO codeword required to achieve the desired output frequency. As the DCO output frequency is very susceptible to PVT variations, such variations should be taken into account in predicting the DCO codeword.

A. PVT Variations of the DCO and the PVT Sensor

Fig. 1(a) depicts a delay-chained oscillator, which used as a DCO, of which cycle period is controllable by a digital codeword, and Fig. 1(b) depicts a ring oscillator that has no special features to control its cycle period. As the cycle period of the fixed ring oscillator is dependent on the PVT variations, it can be used as a sensor to detect the variations. Using the fixed ring oscillator as a PVT sensor, we can detect the

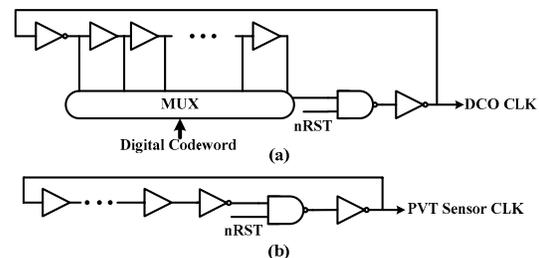


Figure 1. Two oscillators: (a) DCO and (b) PVT Sensor.

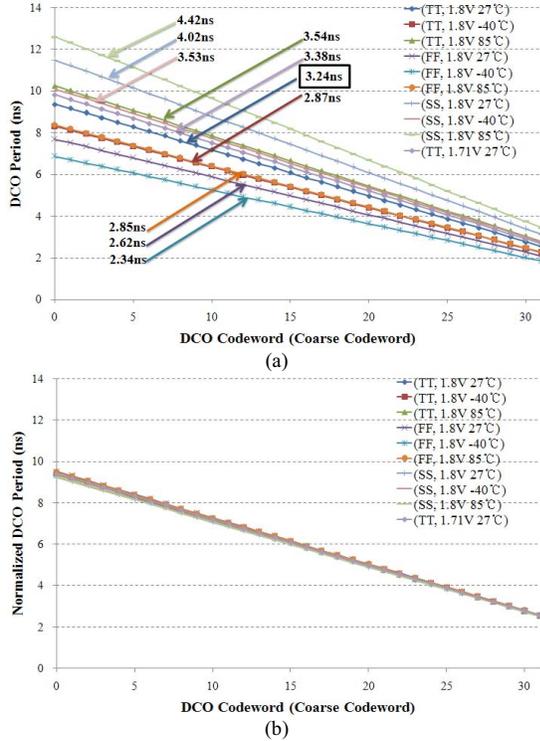


Figure 2. (a) Relationship among DCO Period, operating conditions, and PVT Sensor periods (b) Normalized version of (a).

combined variations by measuring its cycle period. Though we cannot separate each variation, such functionality is not needed in deciding a digital codeword to be used to control the DCO, as we can assume that the DCO and the PVT sensor experience the same variations if they are closely located on a chip. Fig. 2(a) shows a graph that represents the relationship between the DCO period and the DCO codeword, which is generated by considering various operating conditions. More specifically, three process variations are taken into account to include slow (SS), typical (TT) and fast (FF) processes, the supply voltage varies from 1.71V to 1.8V, and the temperature variation ranging from -40°C to 85°C is covered. In addition to this, Fig. 2(a) shows how the PVT sensor period is changing according to the operating conditions. By taking the operating condition of (TT, 1.8V, 27°C) as the reference condition, the graph is normalized using the following equation, as shown in Fig. 2(b).

$$T_{DCO}^{Norm} = T_{DCO}^C \times (T_{Sen}^R / T_{Sen}^C) \quad (1)$$

where T_{DCO}^{Norm} is the normalized DCO period, T_{DCO}^C is DCO period at current condition, and T_{Sen}^R and T_{Sen}^C are the PVT sensor periods at the reference condition and the current condition, respectively. In Fig. 2(b), we can find a fact that the normalized DCO periods coincide into a single line approximately. In fact, the normalized lines fall into one line with an accuracy of 1.6% discrepancy. This fact is quite natural because the DCO and the PVT sensor are experiencing almost the same variations as mentioned before. The fact enables us to predict the DCO codeword by using only the relationship between the DCO codeword and the DCO period

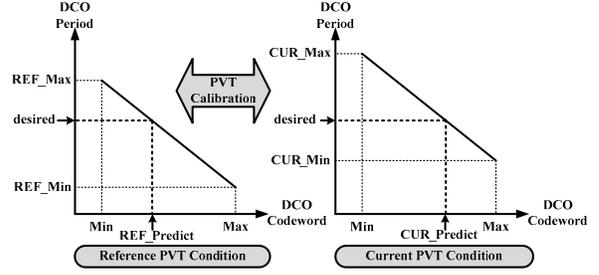


Figure 3. PVT Calibration. (a) Reference PVT Condition (b) Current PVT Condition.

at the reference condition and the PVT sensor period at the current operating condition.

B. PVT Calibration

From the above discussion, we know that the effect of PVT variations to the DCO period can be estimated indirectly by measuring the period of the PVT sensor. As the PVT sensor is a ring oscillator running very fast, it is extremely difficult to measure its period accurately. Therefore, a practically possible solution is to measure the frequency of the PVT sensor instead of the period. For this case, as shown in (2), we derive a new equation that calculates the DCO period at the current condition using the DCO period at the reference condition and the PVT sensor frequency.

$$T_{DCO}^C = T_{DCO}^R \times (F_{Sen}^R / F_{Sen}^C) \quad (2)$$

where T_{DCO}^R is the DCO period for a DCO codeword at the reference condition, and F_{Sen}^R and F_{Sen}^C are the PVT sensor frequencies at the reference condition and the current condition, respectively.

The concept of the proposed PVT calibration is shown in Fig. 3. Let us assume that the DCO period for each DCO control codeword and the PVT sensor frequency at the reference condition are known by performing spice simulations. For the desired DCO period, which is the inverse of the desired output clock frequency, we obtain the DCO control codeword by looking up the linear line obtained at the reference condition, as shown in Fig. 3(a). Then the ratio of the reference PVT sensor frequency to the current frequency of the PVT sensor is multiplied to result in the DCO period to be used at the current condition. This multiplication has the same effect as adjusting the linear line for the current condition, as shown in Fig. 3(b).

C. Interpolation of DCO Period with PVT Calibration

Since the DCO period is approximately linear to the DCO codeword as shown in Fig. 2, it is not necessary to remember all the DCO periods each of which corresponds to a DCO codeword. If we know two extreme DCO periods resulting from the minimum and maximum DCO codewords, we can derive the desired codeword by interpolating the two endpoints. Assuming that the DCO codeword represented in n bits ranges from 0 to $1-2^{-n}$, we obtain the following relation.

$$codeword = (T_{DCO}^{C,Max} - T_{desired}) / (T_{DCO}^{C,Max} - T_{DCO}^{C,Min}) \quad (3)$$

where $T_{DCO}^{C,Max}$ and $T_{DCO}^{C,Min}$ are the maximum and minimum DCO periods at the current condition, respectively, and $T_{desired}$ is the desired DCO period. As $T_{DCO}^{C,Max}$ and $T_{DCO}^{C,Min}$ are dependent on the current condition, it is not possible to know them directly. They can be replaced with those obtained at the reference condition as indicated in (2). This substitution results in the following equations.

$$\begin{aligned} \text{codeword} &= \frac{T_{DCO}^{R,Max} \times (F_{Sen}^R / F_{Sen}^C) - T_{desired}}{T_{DCO}^{R,Max} \times (F_{Sen}^R / F_{Sen}^C) - T_{DCO}^{R,Min} \times (F_{Sen}^R / F_{Sen}^C)} \\ &= \left(\frac{T_{DCO}^{R,Max}}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}} \right) - \left(\frac{T_{Sen}^R}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}} \times T_{desired} \times F_{Sen}^C \right) \\ &= A - (B \times F_{Sen}^C) \end{aligned} \quad (4)$$

where $A = \frac{T_{DCO}^{R,Max}}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}}$ and $B = \frac{T_{Sen}^R}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}} \times T_{desired}$.

In (4), A is a constant value that can be obtained by simulating at the reference condition, and B is also a constant value if the desired output frequency is given. Hence, we can predict the DCO codeword by performing one multiplication and one subtraction, as shown in Fig. 4. Since F_{Sen}^C is only an unknown factor, it should be measured on a chip. For A , it can be delivered to the ADPLL at the booting time or can be fixed at the design time. If the output frequency is to be changed, B calculated outside is written into the ADPLL.

D. Sensor Frequency Measurement

To measure the frequency of the PVT sensor, we have to count the frequency for a predetermined time. As the reference input clock is considered to be stable and accurate, its period can be used for the predetermined time. In the prototype design, the reference clock frequency is 10MHz, and thus its clock period is too short to measure the sensor frequency accurately. To measure the sensor frequency more accurately, in other words, to achieve an accuracy of less than 1% error, we count the PVT sensor frequency for 8 reference clock cycles. The sensor frequency measurement is performed always in a background manner, and the recent measurement is used in the proposed prediction when we need to change the output frequency.

III. IMPLEMENTATION

The overall structure of the ADPLL based on the proposed DCO codeword prediction is shown in Fig. 5 [4]. The reference clock counter (RCC) increases by N for each rising edge of the reference clock, while the output clock counter (OCC) increases by one for each rising edge of the output clock. In the lock state, the values of the RCC and the OCC should be equal to each other, and therefore the output clock frequency is N times of the reference clock frequency. As the resolution of the OCC is the period of the output clock, it is not able to detect the phase error less than the period of the output clock. To measure the phase error precisely, a TDC is used to measure the phase error in the resolution of an inverter delay. The unit of the phase error measured in the TDC and

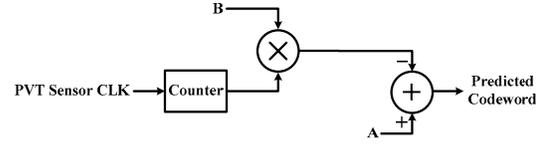


Figure 4. Structure of the proposed DCO codeword predictor.

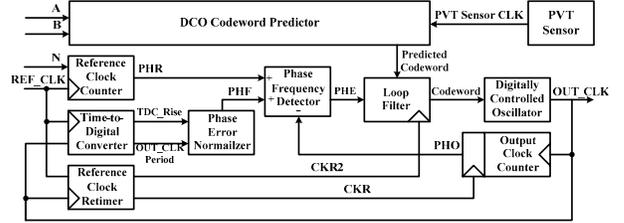


Figure 5. Overall block diagram of the proposed ADPLL.

that of the OCC are different, that is, the former is an inverter delay and the latter is the period of the output clock. To normalize the phase error by the unit of the OCC, the phase error is divided by the period of the output clock. The phase frequency detector (PFD) subtracts the OCC value from the RCC value and adds the normalized phase error to the results. The loop filter (LF) accumulates the PFD outputs and the accumulated value is used to control the DCO. The LF uses the predicted DCO codeword at the first cycle of acquisition.

IV. SIMULATION RESULTS

This section discusses the simulation results for the prototype design implemented in a 0.18 μ m CMOS process. The proposed ADPLL is designed for a system employing the DFS to manage power consumption. The following performance analysis is carried out for output frequencies of 200MHz and 400MHz. For the output frequency of 200MHz, we have considered all the process conditions such as fast (FF), typical (TT) and slow (SS) processes, supply voltage of 1.8V and three temperatures of -40°C, 27°C, and 85°C. For 400MHz, the SS process condition is not taken into account because of the limitation of the DCO frequency range.

A. DCO Codeword Prediction Accuracy

In the proposed technique, the frequency acquisition time is fundamentally determined by the accuracy of DCO codeword prediction. It is necessary to analyze the accuracy of the DCO codeword prediction. For the output frequency of 200MHz, the difference between the predicted DCO codeword and the exact codeword is less than 0.5 coarse codeword when 1 coarse codeword delay is about 150ps. For 400MHz, the difference is less than 0.12 coarse codeword. Therefore, the initial errors of the DCO frequency are at most 3MHz for both of 200MHz and 400MHz output frequencies, leading to less than 1.5% frequency errors.

B. Frequency Acquisition & Lock-in Time

The proposed prediction of the DCO codeword directly contributes to the frequency acquisition time. The proposed ADPLL takes only one cycle to achieve the frequency acquisition when the frequency error of less than 1.5% is the criterion, and the lock-in time ranges from 4 to 20 cycles when

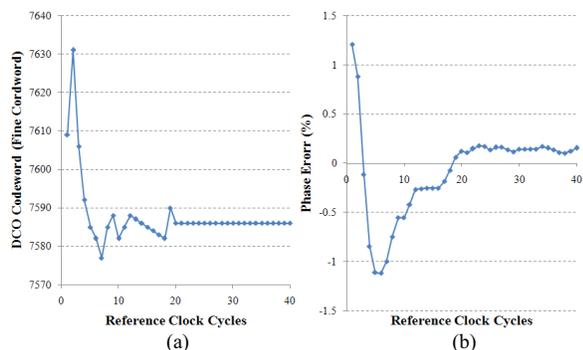


Figure 6. (a) DCO codeword at 400MHz (FF, 1.8V, 27°C), and (b) Phase error at 400MHz (FF, 1.8V, 27°C).

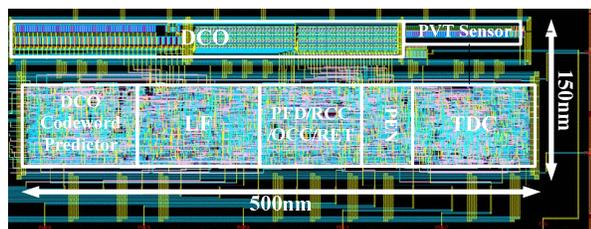


Figure 7. Layout of the prototype ADPLL chip.

the criterion is less than 1.5% phase error. Fig. 6 depicts the codeword and phase error for the output frequency of 400MHz at the condition of (FF, 1.8V, 27°C).

C. Prototype Chip

A layout of the prototype ADPLL is shown in Fig. 7. The core area is 0.075mm² in a 0.18μm CMOS process, and the PVT sensor occupies a much smaller area than the DCO does. In the DCO codeword predictor, most of the area is taken by the interpolation hardware. Compared to [8] employing two inner DCOs each of which occupies 20% of the whole area, the proposed ADPLL reduces a silicon area by about 55% without degrading the performance.

Table I summarizes the characteristics of the proposed ADPLL. The maximum lock-in time is 20 reference clock cycles for various simulation conditions, and the jitter performance is less than 1.5%. The DCO operating frequency ranges from 150MHz to 500MHz. Table II compares the proposed ADPLL with two previous ADPLLs implemented in 0.18μm processes. Among them, the proposed ADPLL shows the smallest area and the fastest frequency acquisition time. The frequency acquisition time of [8] is two-cycles, but it has a large chip area which cannot be ignored. In addition, it does not report the lock-in time and jitter performance. The ADPLL of [2] has a wide output frequency range, but its lock-in time is much longer than that of the proposed ADPLL.

V. CONCLUSION

To achieve fast frequency acquisition for ADPLLs, this paper has presented a new method that predicts the DCO codeword. To compensate the PVT variations, a simple ring oscillator called a PVT sensor is employed. By monitoring the frequency of the PVT sensor, we can easily calculate the DCO codeword necessary to make the DCO oscillate at the desired

TABLE I. CHARACTERISTICS OF THE PROTOTYPE ADPLL

Process	0.18μm CMOS
Frequency Acquisition	1 cycle
Lock-in Time	4-20 cycles
Jitter Performance	1.5%
Output Frequency	150 - 500MHz
PVT sensor + Predictor Area	0.015mm ²
Total Area	0.075mm ²

TABLE II. COMPARISON WITH PREVIOUS WORKS

Design	Proposed (simulation)	[8] (simulation)	[2] (measurement)
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Frequency Acquisition	1 cycle (< 1.5%)	2 cycles	Not reported
Lock-in Time	< 20 cycles (< 1.5%)	Not reported	< 75 cycles
Jitter Performance	1.5%	Not reported	2.8%
Output Frequency	150-500MHz	140-1030MHz	2.4-378MHz
Area	0.075mm ²	0.28mm ²	0.16mm ²

frequency. The proposed prediction approach enables single-cycle frequency acquisition and is superior to the other approaches such as binary searching. Since the prediction can be performed using a ring oscillator and a simple interpolation circuit, the proposed method has an advantage over the previous works, especially over [8] that uses two additional inner DCOs to predict DCO codeword. It is important to note that the DCO period graphs for various operating conditions are converted to only one DCO period graph at the reference condition by taking into account the PVT sensor frequency changes. In addition to the single-cycle frequency acquisition, the prototype design implemented in a 0.18μm CMOS process reduces area by about 55% compared to [8].

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