A 6Gbps SSD Controller using Low-complexity and Time-interleaved BCH Encoder/Decoder

Youngjoo Lee, Hoyoung Yoo, Injae Yoo and In-Cheol Park
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology
yjlee.ics@gmail.com

I. INTRODUCTION

Due to the development of technology, the processing speed of the memory and the processor become faster than ever, however, that of the mechanical storage, which is relatively slow, has been unable to satisfy the requirement of the speed and performance in several areas. The advent of SSD considers the most promising solution to solve the performance difference in those systems because SSD has many advantages, such as fast access time, small size, low-power, etc. This paper proposes a novel SSD controller equipped with low complexity and time-interleaved BCH encoder and decoder.

II. ARCHITECTURE OVERVIEW

Figure 1 shows the proposed SSD controller, where 32-bit Core-A processor [1] is integrated to control the overall process. Generally, a SSD controller is dedicated to a specific NAND chip or an interface environment, but the proposed SSD controller provides the flexibility for those constraints. Instead of changing the whole SSD controller, appropriate micro-instructions are updated in the on-chip SRAM. In addition, 4 NAND flash channels are time-interleaved by Flash controller (FCTRL) to achieve high performance. In other words, FCTRL, in which BCH encoder is inherent, rotationally operates for each channel during the same period of the time.

According to the NAND flash memory specification, 32 error bits within the message 1k bytes BCH(8640, 8192, 32) code is used and the parallel factor for both encoder and decoder is set to 32 so that it can support 6Gbps Serial ATA(SATA) 3 specification at 200MHz. This high parallel factor normally demands high area complexity, but the complexity of BCH encoder and decoder in the proposed SSD controller is optimized by applying folding and sharing common substructure techniques [2], [3]. The phase-overlapping BM structure is newly introduced to maximize the folding effects and the single-matrix parallel syndrome calculation can further reduce the hardware complexity of the BCH decoder. To avoid the high congestions at the massive parallel Chien search, the search area of the parallel Chien search is divided to four blocks and the routing congestions are greatly compensated.

III. IMPLEMENTATION RESULTS

The proposed SSD controller is fabricated with 0.13μm CMOS technology and takes 3.08mm² by using 310k gates. The operating frequency can be achieved up to 200MHz. The proposed SSD controller is also implemented in Altera Stratix IV 4SGX230 and tested with 4 NAND flash channels according to ONFI(Open NAND Flash Interface) 2.0.

REFERENCE


This work was supported by Korea Intellectual Property Office (KIPO) and IC Design Education Center (IDEC).