A 5-GHZ SELF-CALIBRATED I/Q CLOCK GENERATOR USING A QUADRATURE LC-VCO

Hyung Ki Ahn[1], In-Cheol Park[1], and Beomsup Kim[1,2]

[1]Department of Electrical Engineering and Computer Science
Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Berkäna Wireless, Inc., San Jose, CA, USA

ABSTRACT

This paper describes a self-calibration technique to generate precise I/Q signals for frequency synthesis. The phase comparator compares the in-phase signal to the quadrature signal in the quadrature LC-VCO and the charge-pump circuit produces the correction voltage. To verify the functionality of the proposed scheme, the 5-GHz LC quadrature VCO utilized in 5-GHz band wireless LAN, especially, IEEE 802.11a, is designed. The phase error resulting from calibration is under 2-degree in various device mismatches. The oscillator with calibration achieves –121.5 dBc/Hz at 1 MHz offset and exhibits 10 % tuning range. A prototype frequency synthesizer using the proposed scheme is also designed using a 0.18-μm 1-poly, 6-metal standard CMOS process and verified with schematic simulation.

1. INTRODUCTION

Increasing demands for mobile computers have accelerated the development of wireless LAN systems. While wireless LAN systems in 2.4-GHz ISM bands emerged in the market recently, their data transfer rates are limited to a few Mb/s. To satisfy the needs for higher data-rate wireless LAN systems, a transmission band around 5-GHz is proposed by Federal Communications Commission (FCC) as the unlicensed national information infrastructure (U-NII), and as a European standard, high-performance radio LAN (HIPERLAN) is suggested in the near band. These high-performance systems support the data-rate of 16~25 Mb/s per channel.

The heterodyne architecture has been widely used for wireless receivers but the off-chip filters required for image rejection were the biggest barriers for single chip integration of the whole receiver. There have been several experiments to overcome this limit in various ways [1], [2]. A direct conversion receiver, often called homodyne architecture, can be one of the candidates and is very suitable for monolithic integration because it translates the signal of interest directly from RF to baseband and does not need image rejection filters [3]. This removal of off-chip components can eliminate 50-Ω load driver and reduce power consumption and die area significantly. There are still several problems to be solved in direct conversion receivers such as dc offset, I/Q mismatch, even-order distortion and flicker noise. Especially, I/Q mismatch is the biggest challenge in the implementation of CMOS frequency synthesizer.

This paper describes a self-calibration technique for I/Q generation in frequency synthesis, which is designed for a 5-GHz range wireless LAN receiver [4].

2. PROPOSED ARCHITECTURE

To compensate the derived I/Q mismatch, some analog or digital calibration techniques have been adopted [3], and to make I/Q clock signals less sensitive to temperature and process variation, a self-calibrated PLL with a ring oscillator VCO has been proposed [5]. However, the multi-stage ring oscillator requires large power consumption especially at high frequency operation. Also, the phase noise performance is insufficient for most high-performance wireless data transmission systems.

An LC oscillator with a poly-phase filter would be a low power solution for a high frequency receiver if the component mismatches could be controlled [6]. This architecture overcomes the I/Q mismatch arising from resistor and capacitor mismatches in poly-phase filter by self-calibration method. However, the additional buffers between the VCO and the poly-phase filter and LO buffers needed to compensate the power loss caused by the multi-stage of poly-phase filter become the major drawback of the combined architecture of LC-VCO and the poly-phase filter.

A quadrature LC-VCO can easily generate the I/Q signals at the cost of twice power consumption and twice area [7]. If the LC-VCO is well designed, twice power consumption of two VCOs is not an obstacle compared to the power-consuming buffers used in the combined architecture. An additional advantage of the quadrature VCO is its large signal swing that enables the VCO to drive mixer or prescaler directly. There is still a problem that the mismatch between active and passive devices can induce the VCO to generate I/Q imbalance. If it is possible

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to compensate the effects of the mismatch, the quadrature VCO will become one of the fascinating choices.

Fig. 1 (a) shows the schematic of a quadrature LC-VCO. Let's assume that the DC current of oscillator 2 is bigger than that of oscillator 1 by ΔI. After the Vi- voltage reaches to its peak value, the Vq+ starts to go up as the Vi- voltage goes down. As assumed, the bias current of I1+ΔI flows down to the drain of M2a and makes the Vq+ voltage to go up faster, i.e. the phase of Vq+ voltage is increased. The Vq- voltage also moves in the same way. If ΔI<0, the phase of Vq+ and Vq- is decreased.

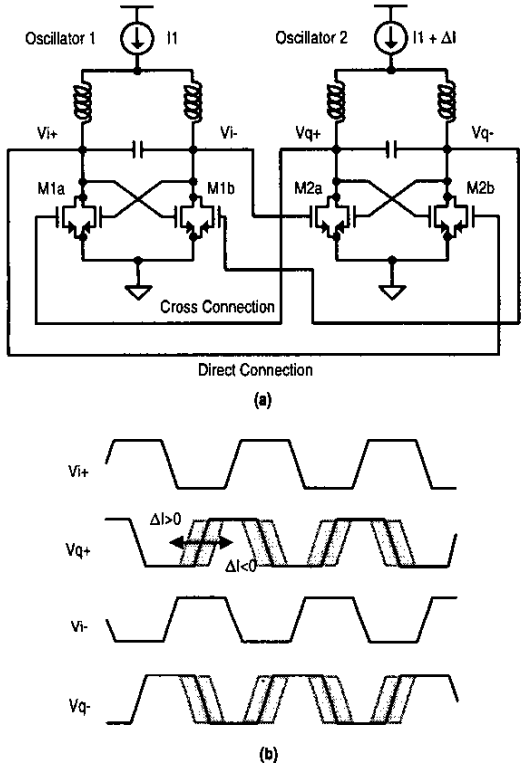

Fig. 1. (a) Quadrature VCO schematic (b) its output waveform

The proposed self-calibration block diagram is shown in Fig. 2 (a), which accepts the four signals, I+, I-, Q+, and Q-, and compares their phase each other. The charge-pump circuit generates the control voltage for the bias current of VCO. The 90-degree phase detector should be used for this purpose, but it is very difficult to implement one operating in high frequency. Therefore, the relative phase comparison in [5] is used. The phase comparator compares region 1 to region 2 as shown in Fig. 2 (b), and the self-calibration loop operates so as to make this difference zero. When the loop locks, a precise 90-degree of phase difference can be acquired.

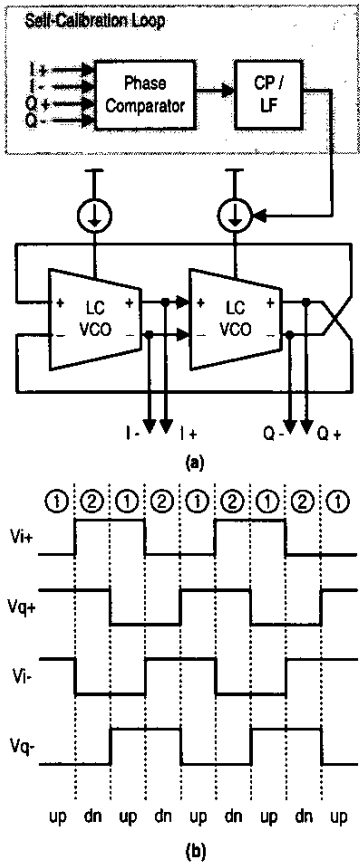

Fig. 2. (a) Proposed calibration method (b) its operation

The frequency synthesizer to confirm the I/Q calibration scheme is designed. As the channel frequency is 20 MHz, quite a large number, an integer-N type frequency synthesizer is selected for this study, which is mainly consisted of VCO, dividers, phase frequency detector (PFD), charge pump and loop filter. To change the wanted channel, a prescaler is necessary. As it is difficult to make a prescaler operating from 5.15 to 5.35 GHz, pre-dividing of 4 is performed before prescaling. Therefore, the reference frequency becomes 5 MHz and the prescaler operates from 1.2875 GHz to 1.3375 GHz.

3. SIMULATION RESULTS

3.1. LC-VCO

As shown in Fig. 1(a), two cross-coupled transistors generate the negative impedance required to cancel the losses of the RLC tank. Usually there should be two times or three times margin of –gm to ensure the oscillation. The inductor model is based on the phi-model of which

parameter is calculated and estimated using the data provided by a foundary. L_s is set to 1 nH.

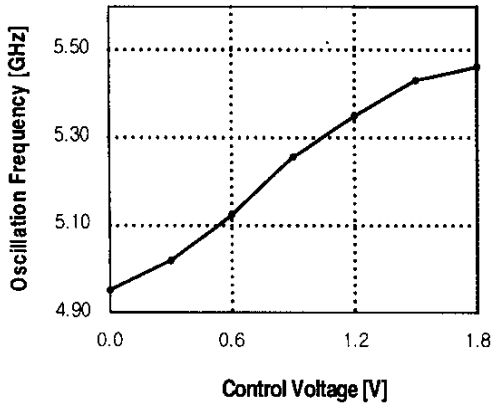

Fig. 3. Tuning Range

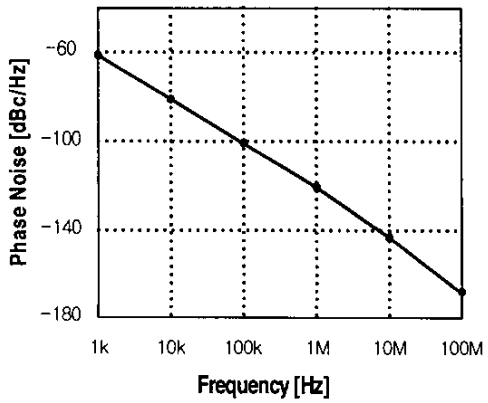

Fig. 4. Phase noise

The varactor model used in this simulation has a polysilicon-oxide-nwell structure called an accumulation-mode MOS capacitor and can change its capacitance by changing the surface population from accumulation to depletion [8].

Fig. 3 and Fig. 4 show the tuning range of simulated LC-VCO and the phase noise simulation results, respectively. The tuning range is from 4.94 GHz to 5.45 GHz and the VCO gain is 286 MHz/V. The phase noise of VCO is measured as −121.5 dBc/Hz at 1 MHz offset when the frequency is 5.3 GHz.

3.2. Calibration Block

The followings show control voltage variation of calibration block when the size variance of input transistors of LC-VCO and the transistors of current source is given. Fig. 5 and Table 1 show the locking behavior of the control voltage and the measured phase error after calibration, respectively.

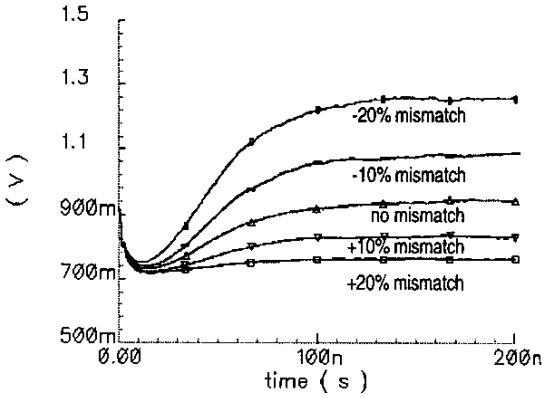

Fig. 5. Locking behavior of calibration loop when the input transistor mismatch occurs

Input Transistor Mismatch	Phase error (degree)	Current Source Mismatch	Phase error (degree)
20%	-1.625	20%	-0.724
10%	-0.862	10%	-0.439
-10%	+0.761	-10%	+0.446
-20%	+1.94	-20%	+0.802

Table 1. Phase error after calibration when the transistor mismatch occurs

The followings show the simulation results when the size variance of inductors in tank circuit is given. Fig. 6 and Table 2 show the locking behavior of the control voltage and the measured phase error after calibration, respectively.

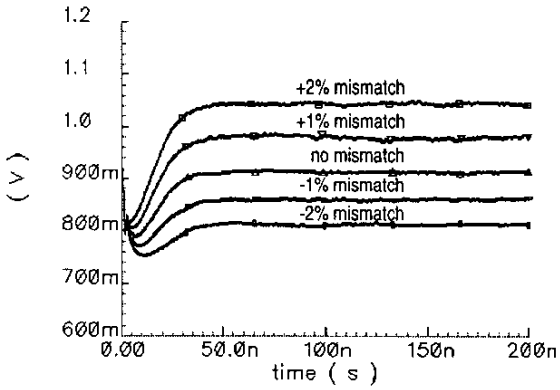

Fig. 6. Locking behavior of calibration loop when the inductor mismatch in tank circuit occurs

Inductor Mismatch	Phase error (degree)
2%	+0.459
1%	+0.359
-1%	-0.212
-2%	-0.267

Table 2. Phase error after calibration when the inductor mismatch in tank circuit occurs

From the above simulation results, it is shown that the phase error can be kept under 2-degree when various device mismatches occur.

3.3. Frequency Synthesizer

The frequency synthesizer is designed as an integer-N type and generates LO signal from 5.18 GHz to 5.32 GHz by 20 MHz spacing. Fig. 7 shows the locking behaviors of the PLL with the proposed calibration block and the calibration loop in the time domain. Fig. 8 shows the output waveform after calibration.

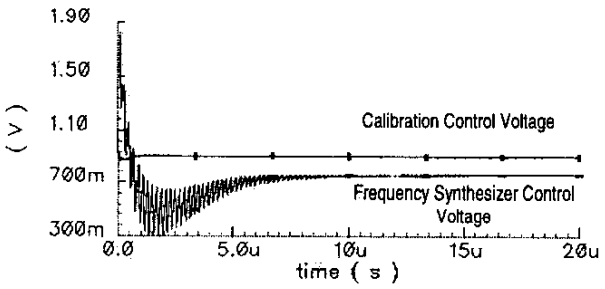

Fig. 7. Locking behavior of closed-loop PLL with calibration

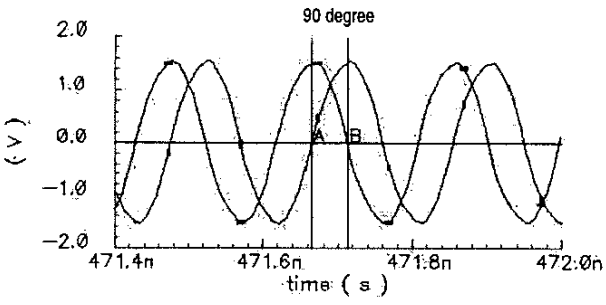

Fig. 8. I/Q signal after calibration

4. CONCLUSION

In this paper, a self-calibration scheme for the quadrature LC-VCO is proposed for I/Q generation. The proposed self-calibration block measures the phase error between in-phase and quadrature signals and corrects them to generate precise I/Q signals. The scheme is developed for 5-GHz band wireless LAN, especially for IEEE 802.11a, and it can be easily adopted to other systems. If we consider the trend to integrate the whole system in one chip, a direct-conversion receiver or image-rejection receiver will be widely used and a precise I/Q generation will become more important.

To verify the proposed scheme, a quadrature LC-VCO and a calibration block are designed using a 0.18-μm 1-poly 6-metal CMOS process. The modeling of on-chip inductor and varactor, which is the critical part of integrated LC-VCO, is based on the data provided by a foundary to acquire reliable simulation results. The designed VCO operates at a sufficient frequency range from 4.94 GHz to 5.45 GHz, which fully satisfies the required tuning range of IEEE 802.11a, and the phase error resulting from the calibration is under 2-degree when the active and passive components have mismatches.

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