A HYBRID DELTA-SIGMA MODULATOR WITH ADAPTIVE CALIBRATION

Jae Hoon Shim[1], In-Cheol Park[1], and Beomsup Kim[1,2]

[1]Department of Electrical Engineering and Computer Science, KAIST, Daejeon, Korea

[2]Berkäna Wireless, San Jose, CA, USA

ABSTRACT

High-order delta-sigma ADCs can achieve wide dynamic ranges at a relatively low oversampling ratio. As high-order modulators may cause instability, a new delta-sigma modulator structure employing hybrid integrators and adaptive calibration is proposed. Hybrid integrators do not suffer from saturation, and they can be applied for high-order modulators without stability problems. The proposed structure uses adaptive calibration to mitigate the performance degradation caused by mismatches between analog and digital paths of hybrid integrators. Behavioral simulations of a fourth-order delta-sigma modulator show that the proposed structure can achieve a significant improvement in dynamic range.

1. INTRODUCTION

Delta-sigma ADCs have been widely used for applications that require wide dynamic ranges such as digital audios [1], and, recently, delta-sigma ADCs have been also used for bandpass sampling of narrow band radio-frequency signals [2]-[3]. This popularity is mainly due to their capabilities achieving wide dynamic ranges with low analog circuit complexity. A typical delta-sigma ADC employs a simple single-bit quantizer. The large quantization noise caused by the single-bit quantizer is suppressed by oversampling and noise-shaping techniques on the band of interest. As oversampling technique limits the signal bandwidth that a delta-sigma ADC can handle, a relatively low oversampling ratio should be used for wideband applications. A wide dynamic range at a relatively low oversampling ratio can be achieved by increasing either the noise shaping order or the number of quantizer levels. The latter requires the use of a prohibitively high-linear multi-bit DAC, while the former often causes instability. To prevent instability, single-stage modulators need gain scaling and clipping of internal signals [4], but this limits the noise shaping performance. Cascading of stable first- or second-order modulators results in high-order modulators with no stability problem, but the cascaded modulator is more sensitive to analog circuit imperfections.

The instability of single-stage high-order delta-sigma modulators is mainly caused by integrator saturation and quantizer overloading. Efforts have been made to overcome these effects [5]-[7]. In [5], the use of local feedback was proposed to return integrators to their normal operating region whenever integrator saturation is detected. Ideally, the local feedback signals should be removed by digital filters, but mismatches between the transfer functions of digital filters and actual signal paths of local feedback signals in the modulator cause leakage. The leakage from the first local feedback loop is most serious because it is not suppressed by noise shaping [6]. Recently, a delta-sigma modulator architecture based on hybrid integrators has been proposed [7]. The architecture is similar to that of [5] but it employs a digital loop filter of different topology. Because the architecture also relies on precise matching of analog and digital paths, appropriate calibration is required. This paper briefly reviews the hybrid delta-sigma modulator architecture and proposes an adaptive calibration method that mitigates the effect of mismatches to improve the performance.

2. HYBRID MODULATORS

Fig. 1 shows a conventional high-order single-stage delta-sigma modulator. It consists of a series of analog integrators and a quantizer. If a single-bit quantizer is used, the quantizer is easily overloaded, leading to instability of the modulator. In addition, the power supply voltage limits the signal range that an analog integrator can handle, and therefore analog integrators easily get saturated, causing harmonic distortions.

A hybrid integrator can cover a wider range of signals than a conventional analog integrator. As shown in Fig. 2, the hybrid integrator is the combination of an analog integrator and a digital accumulator. The input of a hybrid modulator is composed of an analog component and a digital component. The analog component is bounded within [-Vref,Vref]. The overload estimator (OLE) monitors the output of the analog integrator. If the analog output becomes larger (smaller) than Vref (–Vref), the overload estimator decreases (increases) the analog output by 2Vref, and increases (decreases) the digital output by 2Vref instead. As a result, the analog component of the output is also bounded within [-Vref,Vref]. The magnitude of quantization error is always smaller than Vref and quantizer overloading does not occur. Moreover, a hybrid integrator is not saturated provided that the bit width of the accumulator is sufficiently wide.

Generally, a high-order (>2) single-stage delta-sigma modulator using a single-bit quantizer is unstable. However, a stable high-order delta-sigma modulator is possible if hybrid integrators are used in the place of analog integrators, as illustrated in Fig. 3. As hybrid integrators neither suffer from saturation nor cause quantizer overloading, a high-order hybrid delta-sigma modulator based on hybrid integrators is stable although a single-bit quantizer is used. As shown in Fig. 4, the hybrid structure offers a better dynamic range even for second-order modulators because no integrator saturation and quantizer overloading occur. Another advantage of the hybrid modulator is that the use of a multi-bit quantizer does not require a high-linear DAC. The multi-bit quantizer output is fed back to digital paths of hybrid integrators and analog feedback signals are removed altogether.

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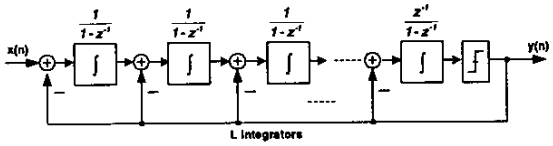

Fig. 1 A conventional delta-sigma modulator

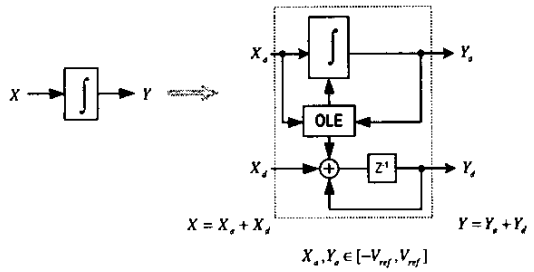

Fig. 2 A hybrid integrator

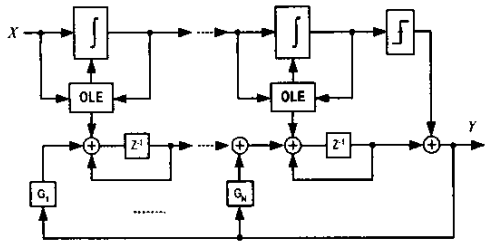

Fig. 3 A hybrid delta-sigma modulator

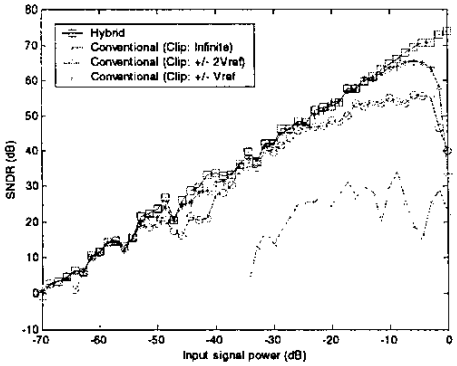

Fig. 4 Performance of second-order delta-sigma modulators

3. CALIBRATION

Although hybrid structures resolve the problem of integrator saturation and quantizer overloading, mismatches exist between the transfer functions of analog integrators and digital integrators. As this may lead to unacceptable performance degradation, calibration is inevitable.

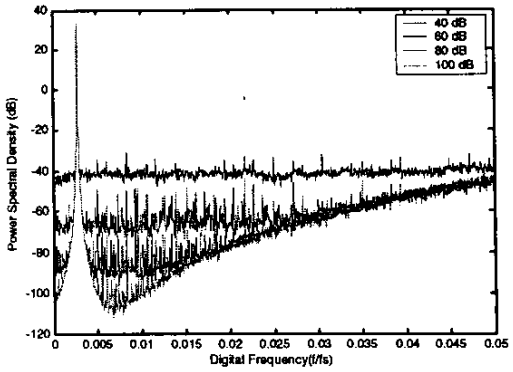

Fig. 5 Typical output spectra of fourth-order hybrid modulators

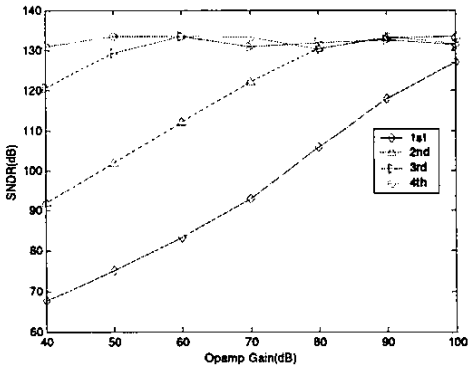

Fig. 6 Peak signal-to-noise-plus-distortion ratios (SNDRs) vs. DC gain of each integrator. Finite gain of the first integrator is most critical

3.1 Mismatches

The transfer function of a digital accumulator is given by

$$Y_d(z) = \frac{z^{-1}}{1-z^{-1}} X_d(z) \qquad (1)$$

Circuit imperfections such as finite DC gain and capacitor mismatches, however, lead to the following transfer function of analog integrators:

$$Y_a(z) = \frac{\beta z^{-1}}{1-\alpha z^{-1}} X_a(z), \qquad (2)$$

where α and β represent the shifts in gain and pole location. This mismatch between the transfer functions leads to imperfect noise shaping and degrades the signal-to-noise ratio. Fig. 5 shows typical output spectra of fourth-order hybrid delta-sigma modulators when the DC gains of op-amps are finite. As

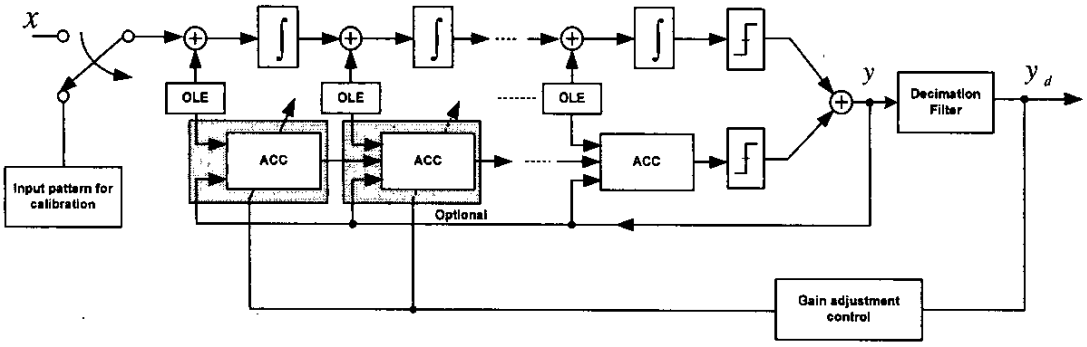

Fig. 7 The proposed calibration scheme

the DC gain decreases, the mismatches and therefore the in-band quantization noise increase. Fig. 6 plots the peak signal-to-noise-plus-distortion ratios (SNDRs) of four fourth-order hybrid delta-sigma modulators, each of which has finite op-amp gain only in the integrator indicated in the figure. As indicated in Fig. 6, the first integrator has the most critical effect on the performance. Consequently calibrating only the first integrator can result in significant improvement.

3.2 Calibration

Minimizing the differences between analog and digital integrators is important in hybrid modulator structure. While controlling an analog integrator so that its transfer function matches that of the corresponding digital integrator is difficult, controlling the digital integrator is relatively easier and more reliable. Once the mismatches are removed, the modulator is equivalent to a conventional single-stage modulator except that it does not suffer from stability problems. Although the transfer functions of integrators are not ideal, the effect on the overall performance is not serious.

Fig. 7 illustrates the block diagram of the proposed calibration scheme. The decimation filter output is monitored and the digital integrators are controlled so that the signal-to-noise ratio (SNR) of the decimated output is maximized. To ease the SNR measurement, a special input pattern is used. If only the quantization noise exists on the band of interest, the measurement of noise power would be rather easy, and the calibration can be performed such that the noise power is minimized. Therefore, the input pattern should not generate any signal component at the decimated output. At the same time, the input pattern should have sufficient power so that overload estimators are activated. An impulse train whose fundamental frequency lies on the out-of-band meets these requirements perfectly and its on-chip generation is easy. As the decimated output does not contain any signal component, the in-band quantization noise can be estimated by

$$P_Q = \frac{1}{N}\sum_{n=0}^{N-1}|y_d(n)|^2 - \left|\frac{1}{N}\sum_{n=0}^{N-1} y_d(n)\right|^2 \qquad (3)$$

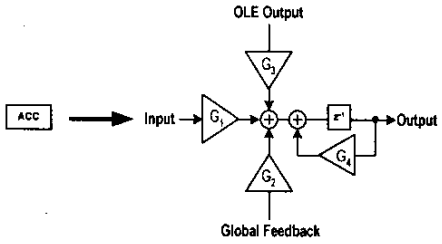

Fig. 8 A digital integrator (accumulator) under calibration

Fig. 8 shows a digital integrator under calibration. The gain coefficients G_1, G_2, G_3 and G_4 are introduced to model the nonidealities of the analog integrator. Let $\underline{g}$ be a vector given by $\underline{g} = [G_1\ G_2\ G_3\ G_4]^T$. It is updated by the steepest descent method based on the following equation:

$$\underline{g}(n+1) = \underline{g}(n) - \mu \nabla P_Q, \qquad (4)$$

where $\nabla = \left[\frac{\partial}{\partial G_1}\ \frac{\partial}{\partial G_2}\ \frac{\partial}{\partial G_3}\ \frac{\partial}{\partial G_4}\right]^T$ and μ is a step size. Equation (4) adjusts $\underline{g}$ such that the in-band quantization noise P_Q is minimized.

4. SIMULATION RESULTS

The proposed calibration method was applied to a fourth-order hybrid delta-sigma modulator. The DC gains of op-amps were all 60 dB and the capacitor mismatches of 1 % were assumed. The oversampling ratio was 64. Fig. 9 shows an example of the quantization noise profile as a function of digital integrator coefficients, G_2 and G_3. The coefficients were adjusted by the steepest descent method. Fig. 10 shows learning curves obtained from behavioral simulations. The coefficients converged after about 30 iterations. Fig. 11 plots the SNDRs as a function of input signal power. Because integrator saturation did not occur, SNDR degradation near the full-scale input was not observed. When first two integrators were calibrated, the peak SNDR was

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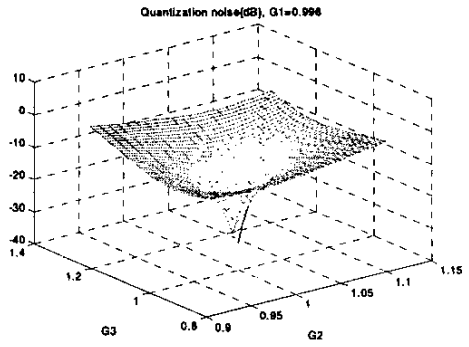

Fig. 9 Quantization noise vs. digital integrator coefficients

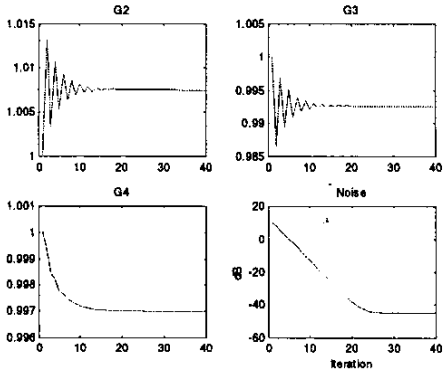

Fig. 10 Learning curves when only the first integrator was calibrated. G_2, G_3, and G_4 are the coefficients of the first digital integrator.

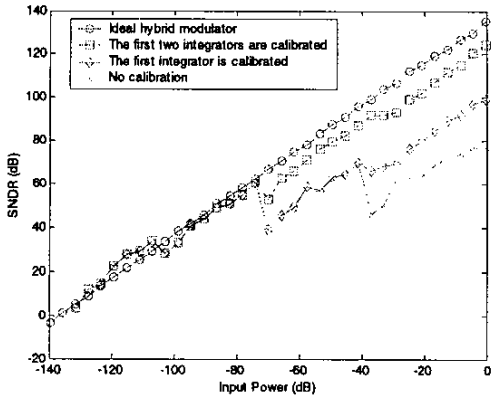

Fig. 11 Calibration performance

120 dB, which is slightly less than that of the ideal hybrid modulator. Comparing with the results when calibration was not applied, calibrating only the first integrator also resulted in significant improvement in SNDRs. Calibrating only a small number of integrators reduces the complexity of the modulator and calibration control hardware, while performance degradation is not serious.

5. CONCLUSION

The main causes of instability of high-order delta-sigma modulators are integrator saturation and quantizer overloading. Delta-sigma modulators employing hybrid integrators do not suffer from these problems because hybrid integrators can handle arbitrarily large input signals by increasing the bit width of digital integrators. Unfortunately, mismatches between analog and digital paths are detrimental to the performance of hybrid modulators. The shortcoming can be overcome by adjusting the coefficients of digital integrators. The proposed calibration method adjusts the digital integrator coefficients to make the transfer function of the digital integrator equal to that of the analog integrator. Simulations showed that a dynamic range of 120 dB at the oversampling ratio of 64 is possible by applying the proposed calibration technique to a fourth-order single-stage hybrid delta-sigma modulator. The drawback of the proposed modulator is the increased digital hardware complexity, but the overhead can be minimized by technology scaling and careful designs of digital circuits.

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