Design of Efficient Embedded System

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I. INTRODUCTION

Recently, a fully-integrated embedded system becomes popular for portable devices due to the cost reduction and the low-power operation. To reduce the size of the embedded program, some hardware techniques such as nop-before-execution and programmable-delay-slot are introduced in Core-A embedded processor [1]. However, the previous designs using Core-A processor are not user-friendly due to the absence of essential environments including the debug solution [2-4]. In this paper an efficient embedded environment using Core-A processor is presented. By introducing a new high-performance Core-B system bus and a monitor based on-chip debug system, proposed embedded system is more attractive to system developers.

II. ARCHITECTURE OVERVIEW

Fig. 1 shows the proposed embedded system. Core-A processor is adopted to control the overall process. To improve high-performance, instruction and data cache controllers are designed. Proposed cache controller supports direct-mapped cache architecture whose size can be programmable. Virtually tagged physically addressing mode is provided by the optimized TLB and 1-cycle hit operation is guaranteed except for the serial write hit case. In the prototype chip, 4KB-size two cache memories and two 256-entry TLB memories are used. Proposed embedded system contains a tightly coupled on-chip debug system as shown in Fig. 1. As Core-A processor decides executing instructions in ID-stage, the traditional halt-mode debugger cannot provide the exact debug solution. However, proposed on-chip debug system determines debugging points according to valid signals in the processor and only executing instructions can be considered as the comparison points. Proposed on-chip debug system is based on the monitor-mode debug method which generates internal interrupt signal and the processor enters the debug routine to communicate to the host server. As the debug software is optimized by using co-processor instructions, user can easily set debug points and the development time can be greatly reduced. Moreover, other useful components such as on-chip SRAM, bootloader, on-chip timer and interrupt controller are also implemented in the proposed embedded system. A high speed on-chip bus named Core-B system bus is used to integrate overall system.

III. IMPLEMENTATION RESULTS

The proposed embedded system is fabricated with 0.13μm CMOS technology and takes only 2.5mm² by using 332k gates. The operating frequency can be achieved up to 250MHz. The test environment including prototype chip is presented in Fig. 2.

REFERENCE