High-Speed and Low-Latency Decoding of Reed-Solomon Codes

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Abstract — **This paper presents a new decoding structure of Reed-Solomon (RS) codes. To achieve both short latency and fast operation, the summation of the products of syndromes is eliminated and the difference used to calculate the error locator polynomial is incrementally updated. The proposed structure called a dual-line structure can operate as fast as the serial structure and has as short latency as the parallel structure.**

I. Introduction

As Reed-Solomon (RS) codes can correct many errors and have an excellent ability to correct burst errors, the codes are being widely used in many applications. The Berlekamp-Massey (BM) algorithm equations has been much used to decode the RS codes by virtue of less complexity [1-3].

$$\Delta_i = \sum_{j=0}^{i-1} \Lambda_j^{(i-1)} S_{i-j} \quad (1)$$

$$L_i = \delta(i - L_{i-1}) + (1-\delta)L_{i-1} \quad (2)$$

$$\begin{bmatrix} \Lambda^{(i)}(x) \\ B^{(i)}(x) \end{bmatrix} = \begin{bmatrix} \epsilon^{(i-1)} & -\Delta_i x \\ \delta & (1-\delta)x \end{bmatrix} \begin{bmatrix} \Lambda^{(i-1)}(x) \\ B^{(i-1)}(x) \end{bmatrix} \quad (3)$$

$$\epsilon^{(i)} = \delta \cdot \Delta_i + (1-\delta) \cdot \epsilon^{(i-1)} \quad (4)$$

In the parallel structure implementation, the BM algorithm can be completed in *2t* cycles. On the other hand, in the serial structure, each iteration takes *(2t+2)* cycles. While the critical path of the parallel structure consists of two multipliers and several adders, that of the serial structure has only one multiplier and one adder. The parallel structure has a merit in latency, and the serial structure has a merit in speed. In this paper, we present high-speed and low-latency RS decoding scheme.

II. Dual-Line Structure

In the new RS decoder structure, the dual-line structure, the registers have an intermediate $\Delta_k^{(i)}$s that become Δ_ks when $\Lambda^{(i-1)}(x) = \Lambda^{(i)}(x)$. Although $\Lambda^{(i)}(x)$ is changing in each iteration, the relationship can be maintained by properly updating the values of registers. Using this structure, the summation in (1) can be eliminated and thus the critical path can be reduced.

Fig. 1 is its implementation for *t=5*. C registers have $\Delta_k^{(i)}$s and D registers have the correction terms. The values of C registers are defined as $C_k^{(i-1)} = \Delta_{k+i}^{(i-1)}$. Since $\Delta_k^{(i)}$s are updated in each iteration, $C_k^{(i)}$s are also updated in each iteration to maintain that relationship. An un-optimized implementation can lead to *6t* registers. However, a structure in Fig. 1 requires only *4t* registers with the following equations[1]. When

[1] During the review process, a similar idea was published in [4]. The difference is that the structure in [4] needs *6t* registers.

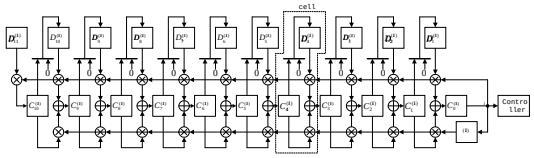

Figure 1: Dual-line RS decoding structure.

i becomes *2t*, we can obtain $\Lambda(x)$ by setting $\Lambda_j = C_j$, for $0 \le j \le t$.

$$C_k^{(i)} = \begin{cases} \gamma^{(i)} \cdot C_{k+1}^{(i-1)} & \text{if } \Delta_i = 0 \\ \gamma^{(i)} \cdot C_{k+1}^{(i-1)} + \Delta_i D_{k+1}^{(i-1)} & \text{otherwise} \end{cases} \quad (5)$$

$$D_k^{(i)} = \begin{cases} 0 & \text{if } k = 2t - i \\ D_k^{(i-1)} & \text{if } k \neq 2t - i \& (\Delta_i = 0 \| 2L_{i-1} > i - 1) \\ C_k^{(i-1)} & \text{otherwise} \end{cases} \quad (6)$$

III. Comparison and Conclusion

It is estimated that the area differences between the structures are small. The critical path of the dual-line structure is the same as that of the serial structure. Since the dual-line structure consists of one cycle, it can generate the error-locator-polynomial in *2t* cycles, which is the same latency as that of the parallel structure. Therefore, the dual-line structure is superior in the view of the delay and the latency with a small hardware increase. In addition, the proposed structure is very regular and easy to implement. The proposed structure can be used in applications that require high-speed and low-latency, such as high-end DVD decoders.

Acknowledgments

This work was supported in part by the Korea Science and Engineering Foundation through the MICROS center, and the Ministry of Science and Technology and the Ministry of Commerce, Industry and Energy through the project System IC 2010.

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