Capacitor Array Structure and Switching Control Scheme to Reduce Capacitor Mismatch Effects for SAR Analog-to-Digital Converters

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Abstract— **This paper presents a new capacitor array structure developed for SAR analog-to-digital converters and its switching algorithm that can alleviate capacitor mismatch effects. The capacitor mismatch can induce many missing codes. The proposed capacitor array structure is based on the junction-splitting method as is efficient in terms of power consumption. To reduce the capacitor mismatch effects, two capacitor arrays are employed to enable redundant search. Simulation results show that the proposed method significantly reduces the number of missing codes caused by the capacitance mismatch, and reduces the energy consumption by more than 70% compared to the conventional charge redistribution method.**

I. INTRODUCTION

The requirements of analog-to-digital converters (ADCs) are dramatically increased in terms of power, speed and resolution, especially for portable applications. Along with the flash ADC [1] and the pipelined ADC [2], the SAR ADC is one of the important topologies widely used for the Nyquist rate ADC. The charge-redistribution SAR ADC proposed in [3] is being actively used in many areas due to its simple control scheme. However, the conventional charge-redistribution method is not efficient in terms of energy consumption since all the capacitors are considered in the process of charging and discharging. As the dominant power of the SAR ADC is consumed during the switching process in the capacitor array, many papers have suggested energy-efficient capacitor array architectures and their switching methods such as the charge sharing method [4] and the capacitor splitting approach [5] [6]. Recently, a new structure referred to as junction-splitting (JS) capacitor array was proposed in [7] to reduce the energy consumed in the capacitor array. By incrementally adding capacitors to generate the comparison voltage, the JS method can reduce about 75% and 60% energy compared to the charge-redistribution method and the capacitor splitting array method, respectively.

When the SAR ADC is implemented based on the capacitor array, the linearity of the ADC is heavily affected by the mismatches among capacitors. Some error correction algorithms have been reported recover the linearity of the DAC. The recent analysis on redundant search [8] [9] reveals that providing multiple paths to a final node can be effective for error correction. The previous redundant search algorithms have focused on the conventional capacitor array architecture,

which means that the capacitor mismatch is regarded as being relatively small because all the capacitors are involved in the charging and discharging process.

As the JS architecture incrementally increases the capacitance to generate the next voltage to be compared, the most significant bit (MSB) is determined with the smallest capacitance value, which means that the JS capacitor array has a chance to be significantly affected by the mismatch of the small capacitors. Applying the traditional redundant tree search to the JS capacitor array straightforwardly would increase the total capacitance significantly and consume more power than the original JS method does. In this paper, we propose a new capacitor array structure that enables the redundant search. Compared to the previous JS structure, the proposed scheme dramatically reduces the missing codes caused by the capacitor mismatch without much increasing the switching power consumption. The rest of this paper is organized as follows: Section II briefly introduces the previous works, and Section III explains the proposed method. Simulation results are analyzed in Section IV, and concluding remarks are made in Section VI.

II. PREVIOUS WORKS

Fig. 1 shows the overall block diagram of an *n*-bit SAR ADC that uses a capacitor array. In the conventional SAR ADC based on the binary search, control signals in Fig. 1 correspond to the *n*-bit decision result. At the beginning stage, switch S_1 is closed to make all the capacitors sample the input voltage, V_{in}. Starting from the most significant bit (MSB), one bit of the final *n*-bit value is determined at a time in the binary search, and thus the conventional SAR ADC takes n cycles to decide the final n-bit value. In the first decision cycle, all control bits to the DAC except the MSB are set to zero to generate the first comparison voltage of $1/2V_{ref}$. In the next cycle, the previous MSB control bit is switched according to the comparison result and the next bit is changed to one. This process is repeated until it reaches the least significant bit (LSB). The status of the conventional DAC capacitor array after sampling the input voltage is shown in Fig. 2. The *0* or *1* denoted at the control line represents a connection to the ground or the reference voltage, respectively. The output voltage in the ith-step is

$$V_{out} = -V_{in} + \frac{C_{Hi}}{C_{Hi}+C_{Li}}V_{ref}$$

(1)

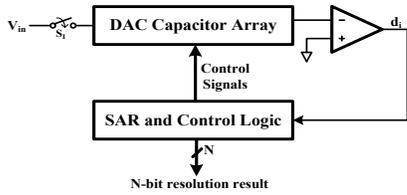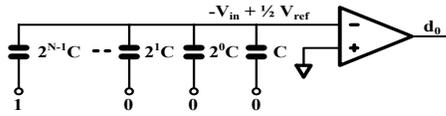Fig. 1. Block diagram of the SAR ADC.

Fig. 2. Conventional capacitor array.

Fig. 3. Junction splitting capacitor array. (a) Conceptual block diagram of the JS SAR ADC. (b) The ith sub-capacitor section of the JS array.

where C_{Hi} and C_{Li} represent the capacitance connected to the reference voltage and ground at the ith-stage, respectively. Therefore, the comparison voltage V_{out} is determined by the capacitance ratio of C_{Hi} to the total capacitor C_{Tot}. As C_{Tot} is constant in the conventional capacitor array, some of the charging processes are wasteful if the corresponding control lines are switched from 1 to 0 during the decision process.

To overcome such power inefficiency, a new capacitor array architecture called junction-splitting (JS) capacitor array has been presented in [7]. Fig. 3(a) illustrates a conceptual diagram of the JS capacitor array structure. The JS capacitor array consists of multiple sections, and the ith section contains i capacitors as shown in Fig. 3(b). The switches for the initial sampling phase are not depicted in Fig 3 for the sake of simplicity. Note that the top plates of the sections are serially connected through additional switches. Compared to the conventional capacitor array in which all the capacitors are involved in generating a comparison voltage, the JS capacitor array generate the voltage by serially connecting the next section. Note that C_{Tot} increases two times at every step and all the capacitors whose control lines are set to 1 are accumulated to derive C_{Hi}. As there is no case that switches any control line from 1 to 0 in the JS capacitor array, the energy consumed in the decision process is theoretically minimum, which is contrast to the conventional architecture that can switch the control lines frequently depending on the input value. In case of a 3-bit ADC, the JS method reduces the energy consumption to one-seventh of the conventional architecture, and in case of a 10-bit ADC, it can reduce to one-fourth on the average [7].

Though the JS method is effective in reducing energy consumption, it is subjective to the capacitance mismatch especially for a few earlier steps in which the total capacitance is relatively small. In the earlier steps, the total capacitance of the JS method is much smaller than that of the conventional array, which means that the JS method is easily affected by a small capacitor mismatch. Due to the small mismatch between unit capacitors, the value of V_{out} can be different from the desired voltage and thus the comparison may result in a wrong decision during the first few stages. As the binary search algorithm never overcomes such an erroneous decision, it is possible to have many missing codes. To recover such errors resulting from the capacitor mismatch, multiple paths should be provided for every final decision value.
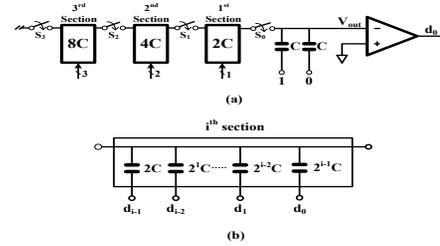
III. PROPOSED ARCHITECTURE AND SWITCHING METHOD

A. Redundant search in SAR ADC

The redundant search allows multiple paths to overcome the wrong decision made in the earlier steps. Compared to the binary search algorithm taking n steps for n-bit decision, a redundant search algorithm needs more steps because of some redundant steps. Although the redundant search is associated with additional clock cycles, the error correction property sometimes enables faster circuitry, shortening the overall conversion latency. Moreover, high accuracy required for analog circuits such as comparators and operational amplifiers can be relaxed by accepting recovery at the later steps [9]. However, the previous redundant search algorithms take into account only the conventional capacitor array architecture and they do not fit well for the JS method. For example, let us consider the 5-bit 6-step redundant search tree shown in Fig. 4, which is constructed by using the generalized algorithm [9]. Note that the earlier three steps offer the recovery paths that may correct wrong decisions. In the JS array, the total capacitance has to be increased in every step. Therefore, the entire capacitance needed to implement the redundant search tree based on the JS method is 4 times larger than that of the original JS method. The 4-times increment is caused by the 8-unit capacitor in the second step. Since the switching energy consumption is directly related to the total capacitance in the capacitor array, a new redundant search algorithm is required to achieve a low-power, mismatch-tolerant SAR ADC. In addition, it is worthwhile maintaining the entire capacitance of $2^n C$ for n-bit precision.

B. Proposed redunadnt search tree algorithm

In order not to increase the entire capacitance, the proposed method employs two capacitor arrays, a main array and a secondary array. For an n-bit SAR ADC, the entire capacitance of $2^n C$ is evenly divided into the main and secondary arrays. The main array plays a major role in decision except the last step, and the secondary array is used to insert redundant nodes to achieve redundant search. In the first two steps, the comparison voltage are provided from the main array, After the second step, the secondary array generates redundant comparison voltages, if necessary, depending on the sequence of the past comparator results. If there is no need to insert an additional comparison step, the main array keeps its previous output voltage for one more clock. In other word, if it is not necessary to check the redundant node, we take two cycles to proceed to the next comparison node. At the final step, two
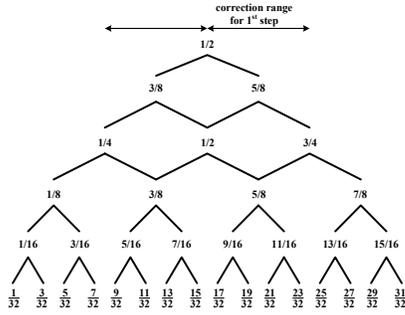
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Fig. 4. *5*-bit *6*-step redundant search tree

Fig. 5. Proposed redundant search tree for a *5*-bit ADC.

capacitor arrays are combined to generate the final comparison voltage. For an *n*-bit ADC, the proposed redundant tree has *n-3* additional steps. Therefore, the final conversion result is obtained in *2n-3* clocks after the initialization phase. For the example of *5*-bit precision, the proposed *7*-step redundant search tree is shown in Fig. 5. We can see two additional steps in Fig. 5, as the proposed method provides *n-3* redundant steps. Note that the comparison nodes denoted with circles are generated by the main array, while the nodes associated with squares are by the secondary array. A dashed line represents a path that takes two cycles to move from the upper node to the following node. At the last step, the main and secondary arrays, both of which are containing *16* unit-capacitors, are connected to derive a comparison voltage that can be achieved with *32* unit-capacitors. Two capacitor arrays and two-cycle paths lead to an efficient redundant tree that can overcome the capacitor mismatch problem. Note that the entire capacitance is the same as that of the original JS capacitor array.

C. Proposed switching method

The conceptual SAR ADC based on the proposed capacitor arrays is shown in Fig. 6. Before reaching the last step, only one of S_{Tm} and S_{Ts} is closed to select a capacitor array. At the last step, both of them are closed to combine the main and secondary capacitor arrays. For *n*-bit precision, the main array structure is exactly the same as the *(n-1)*-bit JS structure. Fig. 7 shows the detailed structure of the secondary array. Four signals are defined to control the two arrays. First, $d_0 d_1 ... d_{2n-4}$ is represents the comparator output sequence and $r_0 r_1 ... r_{n-1}$ is the final conversion code. The *toggle* takes either 0 or 1 to select one of two capacitor arrays and finally, in the secondary array, the control lines of the 1st section, S_{1-1} and S_{1-2}, are defined as follows:

$$S_{1-1} = toggle \wedge (last\_step \,\&\, r_0)$$
$$S_{1-2} = last\_step \,\&\, r_0 \qquad , \qquad (2)$$

where *last_step* is 1 only in the last step. The *toggle* signal is initially zero and becomes 1 when the redundant node should be checked. Fig. 8 depicts the capacitor array structure supporting *5*-bit *7*-step redundant search tree. Note that all capacitors can be controlled with the three terms defined above. Except the last step, if the *toggle* signal is set to 1, S_{Ts} is closed in the odd stages and S_{Tm} becomes 1 in the even stages. If the toggle signal remains 0, S_{Tm} is always set to 1 and S_{Ts} stays 0. Note that both switches are closed in the last step.
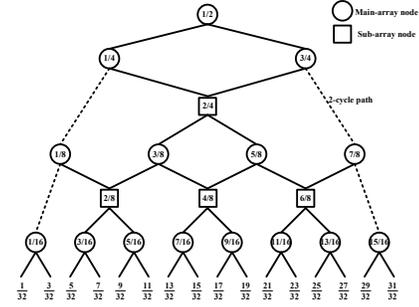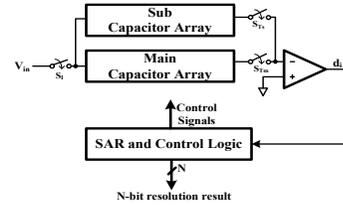

Fig. 6. Conceptual diagram of the proposed SAR ADC.
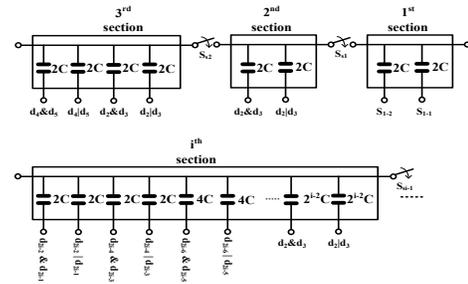

Fig. 7. Detailed structure of the secondary capacitor array.
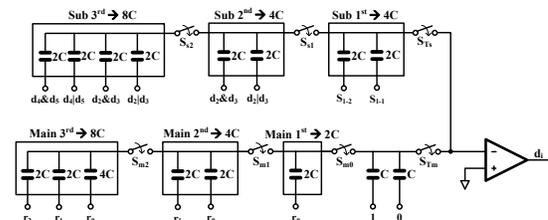

Fig. 8. 5-bit 7-step redundant SAR ADC

The comparison voltage of a redundant node is generated by the secondary array, and equal to the values compared in two steps earlier. The early tested value is generated by the main array by using a half capacitance, as indicated in the denominator of Fig. 5. The comparison voltage generated from the redundant array is more reliable because of the capacitance increased by a factor of two. It is well known that the ratio of small capacitors is more subjective to the mismatch, and thus the capacitance ratio of the redundant node is more reliable than that of the two-step earlier node. To reduce the number of missing codes caused by the capacitor mismatch, we can use the proposed redundant search method only for the first few

steps, if the capacitance of the remaining steps is large enough to guarantee a reliable ratio. For example, a *10*-bit JS SAR ADC can be implemented by employing a redundant capacitor array for the first *5*-bit conversion and an original JS capacitor array for the rest *5*-bit conversion. As the entire capacitance is equal to that of the original JS capacitor array, the proposed configuration is expected to consume almost the same power while reducing missing codes significantly.

IV. SIMULATION RESULTS AND COMPARISONS

Three *10*-bit SAR ADCs have been designed and simulated to compare their switching energy and the number of missing codes caused by capacitor mismatches. The three ADCs are developed based on the conventional capacitor array, the JS capacitor array and the proposed redundant array. For the *10*-bit ADC, the maximum number of redundant steps is 7 in the proposed architecture. Fig. 9(a) shows simulation results on switching energy, where Rx means that x redundant steps are employed in the secondary capacitor array. All the values in Fig. 9 are normalized by the average energy consumption of the conventional ADC. Fig. 9(b) compares the average energy. Since the energy saved from the charge-sharing effect is reduced as the number of redundant steps increases, the average energy dissipated in the proposed architecture increases slightly as the number of redundant steps increases. However, the increment is not significant compared to the average energy consumption of the original JS architecture. Therefore, the redundant array approach still saves about 70% of energy compared to the conventional method.

Fig. 10 shows how many codes are missed when the *10*-bit SAR ADC is subject to capacitor mismatch. Note that almost 10% codes are missed in the full JS array for the case of only 5% capacitor mismatch. By increasing the number of redundant
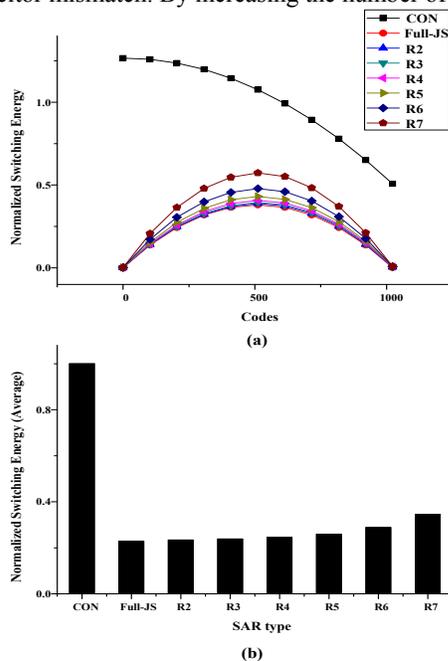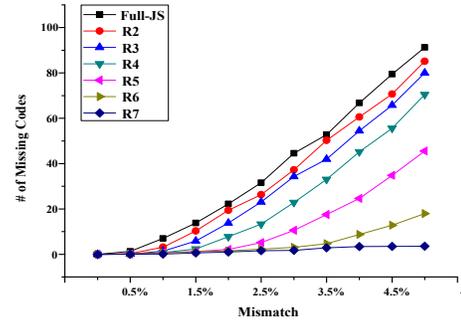

Fig. 10. Missing codes when there is capacitor mismatch in the 10-bit ADC.

steps in the proposed architecture, the number of missing codes is reduced drastically. For 3% capacitor mismatch, for example, we can eliminate about 93% of the missing codes by using 6 redundant steps (R6) and 96% by using 7 redundant steps (R7).

V. CONCLUSION

We have presented a new capacitor array structure and its switching algorithm for SAR ADCs. By applying the proposed architecture, the number of missing codes caused by the process mismatch is significantly reduced without much increasing switching energy compared to the JS capacitor array. An efficient redundant search algorithm suitable for the Junction Splitting algorithm has been proposed and simulated with various redundant steps. The proposed redundant search enabled by two capacitor arrays enhances error recovery significantly against the capacitor mismatch, while maintaining the energy consumption and entire capacitance at the level of the original JS capacitor array.

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Fig. 9. Simulation results on switching energy dissipated in the SAR capacitor array. (a) Energy consumed for each code and (b) average energy.

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