Multiplier-less IIR Filter Synthesis Algorithms to Trade-off the Delay and the Number of Adders

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Abstract

As the complexity of digital filters is dominated by the number of multiplications, many works have focused on minimizing the complexity of multiplier blocks that compute the constant coefficient multiplications required in filters. Although the complexity of multiplier blocks is significantly reduced by using efficient techniques such as decomposing multiplications into simple operations and sharing common subexpressions, previous works have not considered the delay of multiplier blocks which is a critical factor in the design of complex filters. In this paper, we present algorithms to minimize the complexity of multiplier blocks under the given delay constraints and apply them to infinite impulse response (IIR) filter synthesis. By analyzing multiplier blocks in view of delay, three delay reduction methods are proposed and combined into previous algorithms. Since the proposed algorithms can generate multiplier blocks that meet the specified delay, a trade-off between delay and hardware complexity is enabled by changing the delay constraints. Experimental results show that the proposed algorithms can reduce the delay of multiplier blocks at the cost of a little increase of complexity.

1. INTRODUCTION

Infinite impulse response (IIR) digital filters are frequently used in digital signal processing by virtue of low complexity. Although programmable filters based on digital signal processing cores can take an advantage of flexibility, they are not suitable for recent consumer applications demanding high throughput and low power consumption. In such an application, therefore, application specific IIR filters are frequently adopted to meet the constraints of performance and power consumption.

The problem of designing filters has received a great attention during the last decade, as the filters are suffering from a large number of multiplications, leading to excessive area and power consumption even if implemented in full custom integrated circuits. Many works have focused on replacing multiplications by decomposing them into simple operations such as addition, subtraction and shift and reducing the number of simple operations. In this approach, the hardware block called a multiplier block is often used to implement all coefficient multiplications [1]. The concept of the multiplier block is significant in both terms of area and power because some adders and shifters can be shared among different multiplications.

Many algorithms have been proposed to make the multiplier block as simple as possible: Bull-Horrocks(BH) algorithm [2], n-dimensional reduced adder graph(RAGn) algorithm [1], recursive bipartite matching algorithm [3], and common subexpression sharing algorithm [4]. Though the algorithms are proposed for FIR filters, they can be applied to IIR filters [5][6]. The main purpose of these algorithms is to minimize the number of additions/subtractions, as the number is proportional to the number of two-input adders required in the implementation of a multiplier block and the shift can be implemented by wire connections. However, the algorithms do not take into account a factor critical in high performance filters, the delay of the multiplier block, leading to slow filters that may not be suitable for high performance systems.

In this paper, we present new IIR filter synthesis algorithms that are based on our multiplier block synthesis algorithm [7]. Since the proposed algorithm can generate a multiplier block satisfying a given delay constraint, it enables a trade-off between delay and area. In this paper, we propose the application of them to IIR filters. The rest of this paper is organized as follows. In Section 2, the problem to be solved is formally defined, and in Section 3, some basic operations proposed to make the multiplier block meet the specified delay constraint are described. We explain the proposed algorithm and its implementation in Section 4. After we describe the structures of IIR filters in Section 5, we show experimental results in detail in Section 6, and finally conclusions are made in Section 7.

2. PROBLEM DEFINITION

In this section, the problem to be solved will be defined formally. We will start from introducing the following term to be used throughout this paper.

- ***Adder-Step:*** One adder-step represents an adder/subtractor in a maximal path of decomposed multiplications. A multiplication can have different adder-steps, depending on the structure of multiplication.

The problem to be solved is described as follows:

- ***Problem 1:*** Given a delay constraint and a set of filter coefficients, generate a multiplier block satisfying the delay constraint such that the number of adders/subtractors is minimal.

As the delay is dependent on several implementation issues such as circuit technology, placement and routing, we regard in this paper the delay is specified by the number of adder-steps that denotes the maximal number of adders/subtractors allowed to pass though to produce any multiplication. In this case, the above definition is restated as follows.

- ***Problem 2:*** Given a maximal number of adder-steps and a set of filter coefficients, generate a multiplier block that needs a minimal number of adders/subtractors and does not violate the number of adder-steps.

One simple method of achieving the minimum number of adder-steps N is to construct coefficients individually by using a separate

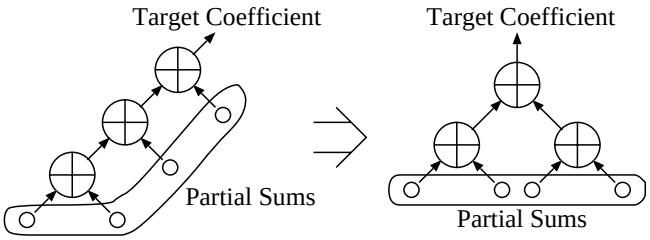

Fig. 1. Tree reduction.

binary tree of adders for each c_i, meaning that adders associated with c_i are not shared with those of other c_j.

3. METHODS FOR REDUCING THE NUMBER OF ADDER-STEPS

In this section, we explain three basic methods that are essential in reducing the number of adder-steps. Our methods are based on BHM[2][5] and RAGn[1][6]. The two algorithms are selected here as they produce the minimal number of adders among many published algorithms.

3.1 Tree Reduction

In constructing coefficients by using the BHM algorithm or the RAGn algorithm, several partial sums are selected and added in a serial manner as shown in the left of Fig.1. It is obvious that the serial structure increases the number of adder-steps. Though the cases do not occur frequently, their effect on the number of adder-steps is significant. To reduce the number of steps for the cases, we can employ a tree reduction technique illustrated in Fig.1. The tree reduction technique is used to convert a serial adding structure to a parallel one.

In applying the proposed tree reduction technique to the BHM algorithm, the sum or difference is put into a temporary set instead of directly putting into the partial sum set. When the synthesis of a coefficient is completed, the partial sums stored in the temporary set are sorted in ascending order of their number of adder-steps, and the partial sums with smaller numbers of adder-steps are added earlier.

3.2 Limited Selection Method

In this and the next subsection, we propose methods to design a multiplier block satisfying a given delay specified by the number of adder-steps. In our investigation on the previous algorithms, we found that a coefficient is synthesized by a series of partial sums and the number of adder-steps for the coefficient is determined mostly by the first pair of partial sums in that series, that is, the adder-steps required to synthesize the first pair of partial sums has a great effect on the final number of adder-steps. If we can start from a pair requiring small numbers of adder-steps in implementing its partial sums, the coefficient can be synthesized with a less number of adder-steps. The basic idea is to select the first pair from a limited set of partial sums whose adder-steps are less than or equal to a given number. An example is illustrated in Fig.2, where the following terms are used.

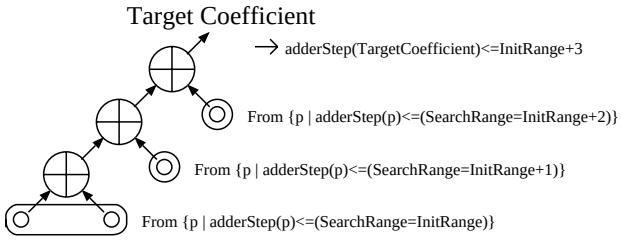

Fig. 2. Limited selection method.

- *InitRange:* the upper limit of the number of adder-steps that the partial sums in the first selected pair can have.
- *SearchRange:* the upper limit of the number of adder-steps that the partial sums selected at that moment can have.
- *CandidateSet:* a subset of partial sums whose number of adder-steps is equal to or less than *SearchRange.*

In Fig.2, the first pair of partial sums shown at the bottom is selected by setting *SearchRange* to *InitRange*. Then the *CandidateSet* is limited to $\{p \mid adderStep(p) \leq (SearchRange = InitRange)\}$, where *adderStep(p)* is the number of adder-steps needed for the partial sum *p*. To select a new partial sum, *SearchRange* is increased by one and the *CandidateSet* is less limited to $\{p \mid adderStep(p) \leq (SearchRange = InitRange+1)\}$. At the next time, *SearchRange* is increased by one again. If a coefficient is to be synthesized with four partial sums as shown in Fig.2, it is guaranteed that the number of adder-steps for the coefficient is less than or equal to *(InitRange+3)*.

The complete description of the limited selection method is as follows. We begin with the maximally allowable *InitRange* that is one less than the specified number of adder-steps, and *SearchRange* is set to *InitRange*. After the first pair is selected, the error between the coefficient being synthesized and the sum or difference of the selected pair is calculated. Then a new partial sum closest to the error is selected with *SearchRange* increased and the error is re-calculated. The selection procedure is iterated until the sum or difference coincides with the coefficient. As mentioned above, *SearchRange* is increased after each selection, and a less limited *CandidateSet* is considered in the later selection. After synthesizing the coefficient, it is examined whether the synthesis of the coefficient meets the specification or not. If not, another iteration is repeated after decrementing *InitRange* i.e. reducing the *CandidateSet* for the first pair. If the iteration reaches to a situation in which *InitRange* is less than 1, i.e., the *CandidateSet* cannot be reduced, we conclude that this method cannot synthesize the coefficient under the given delay constraint. The coefficient given up will be synthesized by the method to be explained in the next subsection.

3.3 Minimum Adder-Step Method

This method is invoked when some coefficients are not synthesized using the above two methods. It is induced from the structure of the minimum number of adder-steps. If we want to synthesize a coefficient with the minimum number of adder-steps, we represent it in the CSD form and add the non-zero digits using the tree structure illustrated in Fig.3. In the minimum adder-step

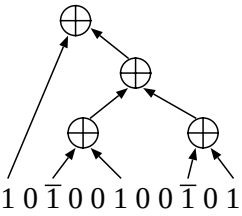

Fig. 3. Adding structure for achieving the minimum number of adder-steps.

method, the procedure for the minimum number of adder-steps is progressed step by step. One of the remained coefficients that do not satisfy the specification is selected, and for convenience let us call the coefficient c_i. A pair of non-zero digits in the CSD form of c_i is selected. Though any pair can be randomly selected, we select two non-zero digits at the lower bit location in our implementation. The value of the pair is calculated and becomes a new partial sum. Next, the methods described in the above subsections are progressed again for the remained coefficients. If coefficient c_i is synthesized with satisfying the specification in the new iteration, another coefficient that is not synthesized with a satisfactory number of adder-steps is selected and a new partial sum is generated by selecting a new pair of non-zero digits in the CSD form of the coefficient. If coefficient c_i does not satisfy the specification in the new iteration, another pair of non-zero digits is selected from its CSD, excluding the previously selected pair. The selected pair becomes a new partial sum and the methods described in the above subsections are processed again. As the procedure is basically the same as synthesizing a coefficient with the minimum number of adder-steps, any coefficient can be synthesized with satisfying the specification unless the specification is less than the minimum number of adder-steps.

4. PROPOSED ALGORITHMS

In this section, we describe two proposed algorithms that can generate multiplier blocks satisfying the given delay constraint. The proposed algorithms are based on three methods of reducing the number of adder-steps and two previous algorithms, BHM and RAGn.

4.1 Step-Limiting BHM Algorithm (SLBHM)

Three methods explained in the previous subsections, tree reduction, limited selection method, and minimum adder-step method, can be combined with the BHM algorithm [2][5]. To synthesize a coefficient, the partial sums selected for the coefficient are put into the temporary set and rearranged by the tree reduction technique. After each synthesis, it is examined whether the synthesis satisfies the specification. If it is, a new synthesis starts for another coefficient. Otherwise, the candidate set where the partial sums are selected is changed by the limited selection method. This is iterated until all coefficients are tried. As stated before, however, the limited selection method does not guarantee the synthesis of all coefficients. If all coefficients are not synthesized, a new partial sum is generated by the minimum adder-step method and the procedure is repeated. We name this algorithm as step-limiting BHM(SLBHM) algorithm.

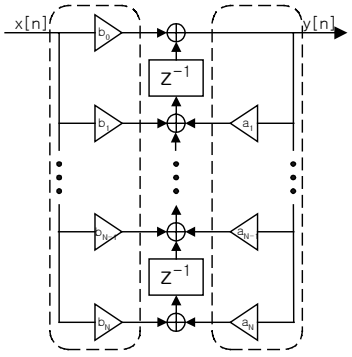

Fig. 4. Direct form II structure of IIR filter.

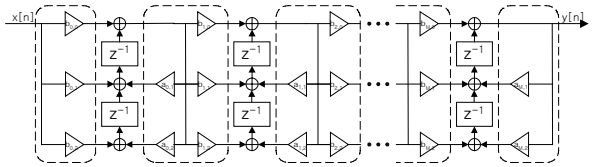

Fig. 5. Cascade form structure of IIR filter.

4.2 Step-Limiting RAGn Algorithm (SLRAGn)

The limitation method can be easily applied to the RAGn algorithm [1][6]. In the optimal part of the RAGn algorithm, the partial sums whose number of adders-steps is less than the specification are searched. If one coefficient is synthesized at the optimal part only using such partial sums, it satisfies the specification. The heuristic part can be divided into two parts: the cost-2 part that requires two adders and the cost-more part that needs more than two adders. As the case that more than two selected partial sums require *(specification-1)* adder-steps is unacceptable in the cost-2 part, such partial sums that make the case are excluded in the selection of partial sums. In order to reduce adder-steps, the cost-more part is replaced by the minimum adder-step method, because the cost-more part is very heuristic and can be replaced by any reasonable procedure. We name this algorithm as step-limiting RAGn(SLRAGn) algorithm.

5. STRUCTURES OF IIR FILTERS

Three commonly used IIR filter structures are direct form, cascade form, and parallel form. The direct form is obtained directly from the system function *H(z)* written as a ratio of polynomials in the variable z^{-1}. The direct form is divided again into direct form Ⅰ and direct form Ⅱ according to whether the parts for zeros are implemented earlier than the parts for poles. The cascade form is achieved by factoring the numerator and denominator polynomials of H(z). It is usually cascaded with several second order filter blocks. When we express H(z) as a partial fraction expansion form, we get the parallel form. It consists of a parallel combination of second order filter blocks. In addition, we can get a transposed form for each form. Fig.4 and Fig.5 shows the transposed direct form Ⅱ and the transposed cascade form respectively, where the multipliers included in a dashed box can be merged into a multiplier block[5].

TABLE I
Test Filter Specification

	w_n	*#tap*	*Width*
Filter 1	0.05	9	8
Filter 2	0.1	7	9
Fitler 3	0.05	7	10
Filter 4	0.1	5	10

TABLE II
Numbers of Adders for Cascade Form Filter 1

#adder-step	Simple	BHM	RAGn	SLBHM	SLRAGn
2	23			21	19
3			18	19	18
4		19			

TABLE III
Numbers of Adders for Cascade Form Filter 2

#adder-step	Simple	BHM	RAGn	SLBHM	SLRAGn
3	27		20	23	20
4		20		20	

6. EXPERIMENTAL RESULTS

The proposed algorithms are applied to several elliptic IIR filters and compared with previous algorithms. The specification of those filters are summarized in Table Ⅰ, where w_n denotes the normalized cutoff frequency, *#tap* is the number of taps, and *Width* is the word size in fixed point integer representation. The ripples of passband and stopband are 0.1dB and 50dB, respectively.

In Table Ⅱ, the results for cascade form of filter 1 obtained by the previous and proposed algorithms are shown. The first row represents algorithms used. 'Simple' means that each coefficient is represented by a CSD value and constructed with a separate binary tree of adders. The first column is the number of adder-steps for the multiplier block optimized by the algorithms identified in the first row and the contents of the table are the number of adders needed to implement the multiplier block. So the BHM algorithm produces a multiplier block of 19 adders and 4 adder-steps and the RAGn algorithm produces one of 18 adders and 3 adder-steps. The SLBHM algorithm produces two multiplier blocks: one is with 21 adders and 2 adder-steps and the other with 19 adders and 3 adder-steps. The SLRAGn algorithm provides two multiplier blocks, too. The one is with 19 adders and 2 adder-steps, the other with 18 adders and 3 adder-steps. Notice that the previous algorithms, BHM and RAGn, give only one result and do not allow to specify the maximum number of adder-steps, while the proposed algorithm, SLBHM and SLRAGn, provide several results under the given delay constraint. In Table Ⅲ, we can see the similar results. Table Ⅳ and Ⅴ show the results for direct form Ⅱ of filters. As the direct form Ⅱ has larger number of coefficients for each multiplier block, the number of adder-steps is larger. The results are similar to the results for cascade form filters. This implies the proposed algorithms enable the trade-off between the number of adders and the number adder-steps, i.e., between the area and the speed.

TABLE IV
Numbers of Adders for Direct Form II Filter 3

#adder-step	Simple	BHM	RAGn	SLBHM	SLRAGn
3	37			27	24
4			21	23	21
5				21	
6				21	
7		21		21	

TABLE V
Numbers of Adders for Direct Form II Filter 4

#adder-step	Simple	BHM	RAGn	SLBHM	SLRAGn
3	30			20	19
4				19	17
5			16	18	16
6		18			

7. CONCLUSIONS

Delay is as important as area. In the previous works, however, only area or the number of adders is considered in implementing and optimizing filters. In this paper, we have described IIR filter synthesis algorithms that take into account the delay and the number of adders. With these algorithms, we can implement filters satisfying the given specification of the number of adder-steps. Contrast to the previous works that generate only one tuple of the number of adders and the number of adder-steps, many tuples are generated in the proposed algorithms, and therefore the trade-off between area and speed is enabled. Experimental results show that the proposed algorithms can reduce the delay of multiplier blocks at the cost of a little increase of complexity.

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