QUADRATURE DIRECT DIGITAL FREQUENCY SYNTHESIS USING FINE-GRAIN ANGLE ROTATION

Sung-Won Lee and In-Cheol Park

Department of Electrical Engineering and Computer Science, KAIST
373-1 Guseong-Dong Yuseong-Gu, Daejeon 305-701, Republic of Korea

ABSTRACT

This paper presents an area- and power-efficient quadrature direct digital frequency synthesis technique called fine-grain angle rotation. To reduce the large bit-width requirement of the angle rotation, multiple start points are introduced and the angle rotation is applied to the small angle remained. A prototype chip occupies 0.16mm^2 in 0.25μm 1P5M CMOS technology and consumes 90mW at 400MHz clock frequency, which is significantly improved performance compared to the previous state-of-the-art chips.

1. INTRODUCTION

The direct digital frequency synthesizer (DDFS) plays a crucial role in frequency agile and spread-spectrum communications systems due to its fast frequency switching capability, continuous phase, fine frequency resolution, and good spectral purity. Most DDFSs are composed of a phase accumulator and a sine/cosine generator [1]. ROM-based lookup schemes are widely used in the sine/cosine generation. As the ROM takes considerable area, several compression techniques were proposed [2]. For the applications requiring high spurious free dynamic range (SFDR) such as tunable digital bandpass filters and mixers for digital receivers, angle rotation schemes based on scalable modular architectures [3, 4] have an advantage that the size increases linearly. However, the angle rotation techniques usually require larger internal bit resolution than the output resolution to prevent the accumulation of round-off errors. The large internal resolution leads to large area and causes more power consumption. An interpolative angle rotation technique [5] was proposed to reduce the resolution requirement. The technique achieves a small reduction of the internal bit resolution but fails to reduce the area and power consumption. In this letter we describe an efficient direct digital frequency synthesis technique called fine-grain angle rotation that reduces internal bit resolution and achieves less area and power consumption.

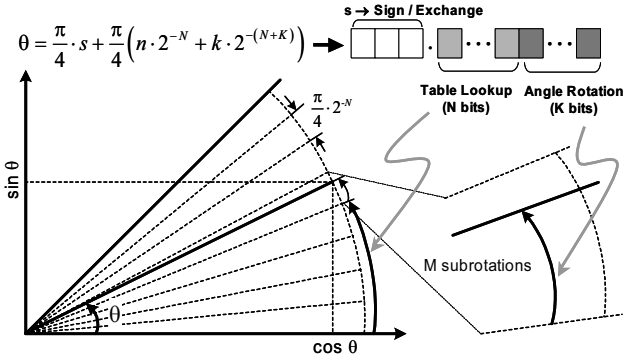


Fig. 1. Basic concept of fine-grain angle rotation

2. FINE-GRAIN ANGLE ROTATION

For a given phase θ, cosθ and sinθ are computed by applying two steps: a table lookup for the coarse phase and an angle rotation for the fine phase remained. As shown in Fig. 1, θ is decomposed into three parts. The first 3-bit part represents the π/4 symmetry exploited to cover any phase in (0, 2π). The second *N*-bit part is the coarse phase to be used to lookup two tables that contain 2^N cosine/sine entries with a bit resolution *L*. The lookup values are start points of the fine angle rotation of the remaining *K*-bit part. Each table entry stores an accurate value of cos $(\pi/4\cdot(n\cdot 2^{-N} + 2^{-N-K-1}))$ or sin $(\pi/4\cdot(n\cdot 2^{-N} + 2^{-N-K-1}))$, where *n* is an integer, $0 \le n < 2^N$ and 2^{-N-K-1} is introduced to compensate the phase gap caused by the π/4 symmetry calculation. While the table size increases exponentially according to the input bit width, it increases linearly according to its output size. Therefore, if we control *N* to be small, the two tables can be implemented without the compression technique [2]. The usage of tables is different from previous angle rotation schemes [4] that reduces a number of initial stages by storing the intermediate values resulted from the initial stages into tables.

Next, an angle rotation is applied to rotate the given start point by $\theta_k = \pi/4 \cdot (k \cdot 2^{-(N+K)})$, where k is an integer, $0 \le k < 2^K$. The CORDIC algorithm [3] can compute the angle rotation by decomposing $\theta_k = \sum_i \sigma_i \cdot \text{atan}(2^{-i})$, where $\sigma_i \in \{-1, 1\}$. As the CORDIC algorithm uses a successive approximation to decide σ_i, the redundant carry-save arithmetic is hardly exploited and additional comparing logic is necessary, impeding a high speed and low-power implementation. Fortunately, the table lookup let θ_k to have N leading-zeros as $\pi/4 < 1$. In this case, the rotation can be computed at a time by determining N and K such that the σ_i prediction scheme [6] becomes valid. Let us consider θ_k with N leading zeros

$$\theta_k = .00\cdots 0 x_{N+1} x_{N+2} \cdots x_{2N+2} \cdots x_{3N+3} x_{3N+4} \cdots. \quad (1)$$

As $\text{atan}(2^{-i}) = 2^{-i} - 2^{-3i}/3 + \cdots$, the prediction of σ_i's is possible by setting $\sigma_i = 1$ for $i = N + 1$, and $\sigma_i = 2(x_{i-1} - 1/2)$ for $N + 1 < i \le 3N + 4$. Therefore, if $K < 2N$, the angle rotation by θ_k can be calculated using σ_i's determined directly from the prediction.

Let $X_{n,N}$ and $Y_{n,N}$ be the lookup values corresponding to the cosine and sine of the coarse phase, respectively. Then the sequence of subrotations are expressed as

$$\begin{aligned} X_{n,i+1} &= X_{n,i} - \sigma_{i+1} 2^{-i-1} Y_{n,i} \\ Y_{n,i+1} &= Y_{n,i} + \sigma_{i+1} 2^{-i-1} X_{n,i} \end{aligned} \quad (2)$$

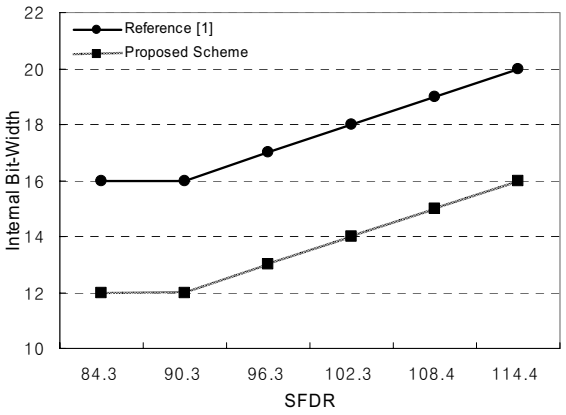
where $N \le i \le 3N + 4$. The values having completed M subrotations, $X_{n,N+M}$ and $Y_{n,N+M}$ can be approximated for $N \ge L/3$ as follows

$$\begin{aligned} X_{n,N+M} &\cong X_{n,N} - Y_{n,N} \sum_{i=N+1}^{N+M} \sigma_i 2^{-i} - 2^{-N-1} \cdot X_{n,N} \sum_{i=N+1}^{N+M} \sigma_i 2^{-i} \\ Y_{n,N+M} &\cong Y_{n,N} + X_{n,N} \sum_{i=N+1}^{N+M} \sigma_i 2^{-i} - 2^{-N-1} \cdot Y_{n,N} \sum_{i=N+1}^{N+M} \sigma_i 2^{-i} \end{aligned} \quad (3)$$

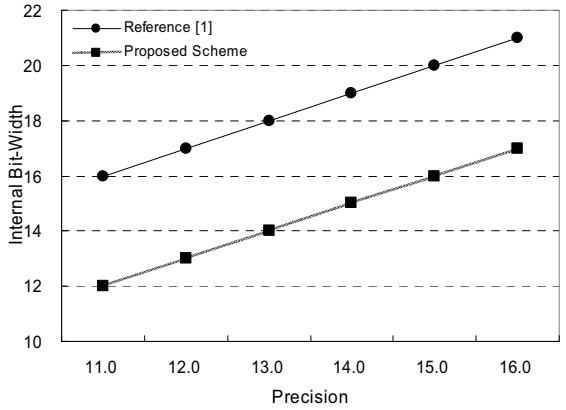
Compared to the approximation in [4], the third term is newly introduced to make the approximation valid for small N, and to improve the precision and the spurious performance as well. Replacing σ_i with $2x_{i-1} - 1$ for $i > N + 1$, we have

$$\begin{aligned} \sum_{i=N+1}^{N+M} \sigma_i 2^{-i} &= 2^{-N-1} + \sum_{i=N+2}^{N+M} (2x_{i-1} - 1) 2^{-i} \\ &\cong \sum_{i=N+1}^{N+M-1} x_i 2^{-i} = \theta_k \end{aligned} \quad (4)$$

which means θ_k can be used in the multiplication directly. The scaling factor [3, 4] is not considered in the above calculation because its effect on the final output is negligible. The simulation result shows that a DDFS designed with $N = 7$, $K = 9$, $M = 10$, and $L = 16$ achieves 15.0 bits precision and 114-dBc SFDR, while a DDFS



(a) SFDR vs bit-width requirement



(b) Precision vs bit-width requirement

Fig. 2. Internal bit-width requirement comparison with respect to SFDR and precision

using 16-stage angle rotation with $L = 16$ has 11.5 bits precision and 91.5-dBc SFDR. To achieve the same performance as the proposed one, the 16-stage angle rotation should have $L = 20$.

Fig. 2 shows how effective the proposed scheme is in reducing the internal bit-width requirement. Experimental results show that the proposed sine/cosine calculation scheme is effective in reducing the internal bit-width. For the same SFDR specification that ranges from 84.3-dBc to 114.4-dBc, the proposed scheme requires 4 bits smaller internal bit-width. It also requires 4 bits smaller internal bit-width to achieve the same precision that ranges from 11.0-b to 16.0-b. The smaller internal bit-width leads to compact design as well as low power consumption.

3. IMPLEMENTATION

The block diagram of the prototype DDFS chip is shown in Fig. 3. A 32-bit phase accumulator is partitioned into two 16-bit carry select adder sections, and its 32-bit output is truncated into 19 bits. The three most significant bits are used to control the direction of input phase and

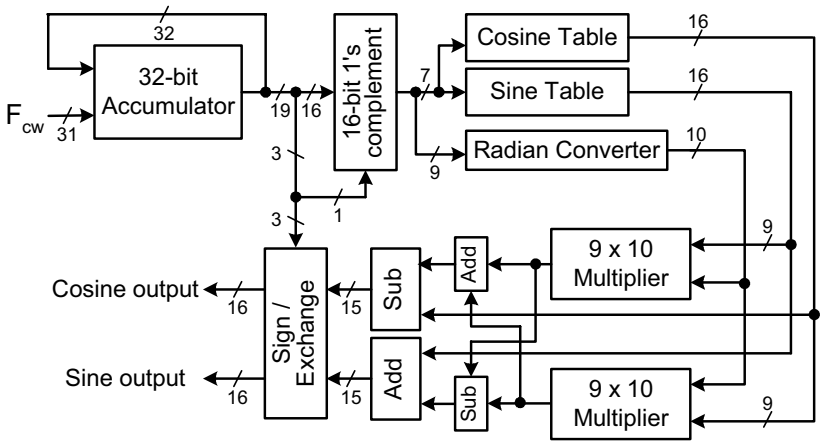


Fig. 3. Block diagram of the prototype DDFS chip

sign/exchange at the output. The 16-bit phase is decomposed into upper 7 bits (N) and lower 9 bits (K). The internal bit resolution L is set to 16 bits to achieve SFDR exceeding 114-dBc. The sine/cosine tables have 128 (2^N) entries of 16-bit values and are optimally synthesized in combinational random logic from a PLA style description. As the 9-bit phase is a normalized value, a radian converter implemented with a simple constant multiplier is employed to obtain a corresponding radian value. The upper 9-bit values of the cosine/sine tables and the 10-bit (M) output of the radian converter are multiplied using two 9×10 unsigned multipliers that employ a Wallace-tree structure and two-stage pipeline. After the final addition/subtraction, 16-bit sine/cosine values are produced.

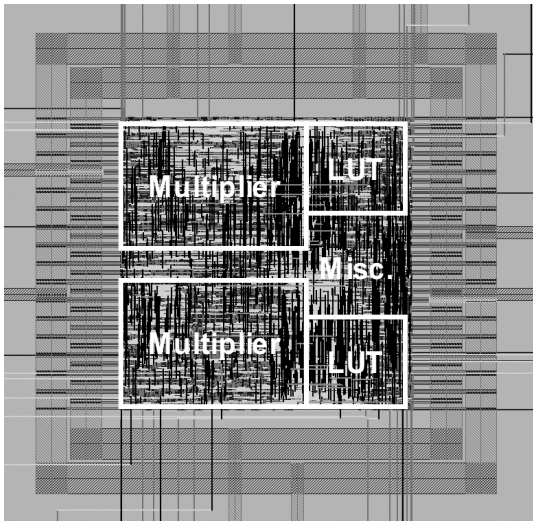


Fig. 4. Layout of the prototype DDFS chip

4. RESULTS

The prototype chip was designed in a 0.25μm 1P5M CMOS technology. Fig. 4 shows a layout of the chip whose active core occupies 0.16mm^2. The maximum operating clock frequency is 400MHz and simulated power consumption is 90mW with 2.5V power supply. The frequency tuning resolution is 0.09Hz. Table 1 summarizes the performance of the proposed DDFS and previous DDFS chips designed for high resolution and spurious performance.

5. CONCLUSIONS

In this paper we have presented a quadrature direct digital frequency synthesis based on fine-grain angle rotation. The proposed technique is effective in reducing large the internal bit resolution of the angle rotation. From the prototype chip design, we found that the technique results in significantly compact design and low-power consumption even compared to the state-of-the-art DDFS chips.

6. ACKNOWLEDGEMENTS

This work was supported by the IDEC and the MICROS center.

7. REFERENCES

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Table 1. Performance comparison with previous DDFS chips

	Nicholas [2]	Madisetti [4]	Song [5]	This work
Process	1.25μm(5V)	1.0μm(5V)	0.35μm (3.5V)	0.25μm(2.5V)
Type	Cosine only	Quadrature	Quadrature	Quadrature
Internal resolution	11 bits	22 bits	18 bits	16 bits
Output	12 bits	16 bits	16 bits	16 bits
SFDR	90.3-dBc	100-dBc	96-dBc	114-dBc
Max clock	150MHz	100MHz	150MHz	400MHz
Power	950mW at 100MHz	1400mW at 100MHz	670mW at 150MHz	90mW at 400MHz
	9.5mW/MHz	14mW/MHz	4.5mW/MHz	0.23mW/MHz
Area	24.5mm^2	12mm^2	3.4mm^2	0.16mm^2

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APPENDIX 1.
DERIVATION OF APPROXIMATION EQUATION

Let $X_{n,N}$ and $Y_{n,N}$ be a starting point of the following angle rotation steps (N: bit-width of the coarse phase, M: number of subrotations). The sequence of subrotations are $X_{n,i+1} = (1 - 1/2\cdot(\sigma_{i+1}2^{-i-1})^2)\,(X_{n,i} - \sigma_{i+1}2^{-i-1}Y_{n,i})$ and $Y_{n,i+1} = (1 - 1/2\cdot(\sigma_{i+1}2^{-i-1})^2)(Y_{n,i} + \sigma_{i+1}2^{-i-1}X_{n,i})$, where $N \le i \le N + M - 1$ and we assume that $\text{atan}(\sigma_{i+1}2^{-i-1}) \approx \sigma_{i+1}2^{-i-1}$ and $(1 - 1/2\cdot(\sigma_{i+1}2^{-i-1})^2)$ is a scale factor [1] that approximates $\cos(\sigma_{i+1}2^{-i-1})$. Putting M scale factor terms into a single term, we have

$$\prod_{i=N}^{N+M-1}\left(1-1/2\cdot\left(\sigma_{i+1}2^{-i-1}\right)^2\right) \cong 1-1/2\sum_{i=N}^{N+M-1}\left(\sigma_{i+1}2^{-i-1}\right)^2 = 1-1/2\sum_{i=N}^{N+M-1}2^{-2(i+1)} \cong 1-2/3\cdot 2^{-2(N+1)} \cong 1-2^{-2(N+1)}$$

Then the first subrotation becomes $X_{n,N+1} = (1 - (\sigma_{N+1}2^{-N-1})^2)X_{n,N} - \sigma_{N+1}2^{-N-1}Y_{n,N}$ and $Y_{n,N+1} = (1 - (\sigma_{N+1}2^{-N-1})^2)Y_{n,N} + \sigma_{N+1}2^{-N-1}X_{n,N}$. The sequence of next subrotations are $X_{n,i+1} = X_{n,i} - (\sigma_{i+1}2^{-i-1})Y_{n,i}$ and $Y_{n,i+1} = Y_{n,i} + (\sigma_{i+1}2^{-i-1})X_{n,i}$ where $N < i \le N + M - 1$. Finally, the output values after M subrotations are

$$X_{n,N+M} \cong (1-T)\,X_{n,N} - Y_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} \quad \text{and}$$

$$Y_{n,N+M} \cong (1-T)\,Y_{n,N} + X_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i}\,.$$

The term T is a summation of the terms shown in Fig. 5.

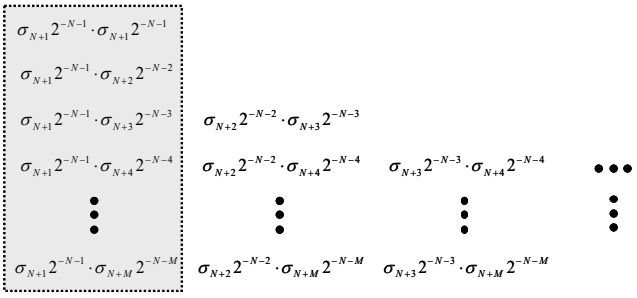

Fig. 5. Approximation of the intermediate term T

From the terms in Fig. 5 we select those in the first column and do not consider the others that are negligibly small. Consequently, we have the approximation equation as follows

$$X_{n,N+M} \cong X_{n,N} - Y_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} - 2^{-N-1}\cdot X_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i}$$

$$Y_{n,N+M} \cong Y_{n,N} + X_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} - 2^{-N-1}\cdot Y_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i}$$