A Third-Order $\Sigma\Delta$ Modulator in 0.18-μm CMOS With Calibrated Mixed-Mode Integrators

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***Abstract*—This paper describes a third-order sigma-delta ($\Sigma\Delta$) modulator that is designed and implemented in 0.18-μm CMOS process. In order to increase the dynamic range, this modulator takes advantage of mixed-mode integrators that consist of analog and digital integrators. A calibration technique is applied to the digital integrator to mitigate mismatch between analog and digital paths. It is shown that the presented modulator architecture can achieve a 12-dB better dynamic range than conventional structures with the same oversampling ratio (OSR). The experimental prototype chip achieves a 76-dB dynamic range for a 200-kHz signal bandwidth and a 55-dB dynamic range for a 5-MHz signal bandwidth. It dissipates 4 mW from 1.8-V supply voltages and occupies 0.7-mm^2 silicon area.**

***Index Terms*—Analog–digital conversion, calibration, sigma-delta modulation.**

I. Introduction

OVERSAMPLING analog-to-digital converters (ADCs) employing noise shaping techniques have been widely used because they provide an effective means to achieve a high resolution without the need for high-precision analog circuits. In particular, single-loop 1-b sigma-delta ($\Sigma\Delta$) ADCs have been popular for their simplicity and insensitivity to imperfections of analog circuits [1], [2]. However, single-loop structures are not attractive for high-order (>2) $\Sigma\Delta$ modulation because of stability concern. Although a single-loop high-order modulator can be stabilized using various techniques, they results in loss of performance, in general. A popular way to realize a stable high-order $\Sigma\Delta$ modulator is to use a multistage or cascaded structure [3]. Cascaded structures, however, are prone to noise leakage due to mismatch among modulators and the noise-cancellation filter, sometimes calling for digital correction [4], [5]. An alternative approach for a stable $\Sigma\Delta$ modulator is to employ a multibit quantizer. The multibit quantizer not only reduces the quantization noise power, but it also improves stability of the modulator. The main drawback of using a multibit quantizer is stringent linearity requirements placed on the feedback digital-to-analog converter (DAC). The accuracy of the DAC needs to be as good as the overall $\Sigma\Delta$ modulator, necessitating digital correction [6] or dynamic element matching [7], [8].

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One important issue that should be addressed in the design of high-order stable $\Sigma\Delta$ modulator is reduced power supply voltages. As supply voltages scale down, the available signal swings of analog circuits decrease, thereby limiting the dynamic range of the $\Sigma\Delta$ modulator and even jeopardizing stability. These problems could be alleviated by means of local feedbacks around loop-filter integrators. Depicted in Fig. 1(a) is the conceptual diagram of the local feedback. The decision block monitors the output and/or the input of the analog integrator. If the integrator is expected to be overloaded or saturated, the decision block subtracts a pre-defined value from the integrator input. Meanwhile, a digital equivalent signal is applied to the digital compensator that simulates the analog path. In this manner, the effective signal swing of the integrator can be increased even if the power supply voltage is reduced.

Several modulator structures employing local feedbacks have been proposed [9]–[12]. Fig. 1(b) shows the architecture proposed in [9]. The overload detector (OLD) keeps track of only the integrator output. If the output of an integrator exceeds a certain level ($V_{\rm ovl}$), the integrator output is likely to exceed the allowed maximum voltage ($V_{\rm max}$), in the next time step. In order to prevent integrator from being saturated, the local feedback loop is activated and the digital counterpart of the feedback signal is applied to digital compensators (H). Modulator coefficients (k, j, and l) and overload voltage ($V_{\rm ovl}$) should meet certain criteria to ensure stability [9]. Since the overload detector uses only the integrator output, it rather overestimates the possibility of integrator saturation. The criteria for modulator coefficients and the overload voltage $V_{\rm ovl}$ can be relaxed for better signal-to-noise ratio (SNR) performance and easier implementation without endangering the stability [10], but finding the optimal set of coefficients is a difficult job.

An alternative structure employs mixed-mode integrators as shown in Fig. 1(c) [12]. The mixed-mode integrator is a combination of an analog integrator and a digital integrator. The modulator can be viewed as a conventional single-loop $\Sigma\Delta$ modulator with analog integrators replaced by mixed-mode integrators. In contrast with Fig. 1(b), no global feedback exists in the analog path since all the global feedback signals are fed to the digital counterpart. As a result, stability of the analog path is readily verified provided that the local feedbacks around the analog integrators work properly. It can be shown easily that the digital path is also stable. The overload estimator (OLE) monitors both the input and the output of the integrator in order to decide whether the integrator would be saturated or not. If the integrator output is expected to exceed $V_{\rm ref}$ for sure, a feedback signal as large as $2V_{\rm ref}$ can be safely subtracted from the integrator input in order to make the integrator output stay in $[-V_{\rm ref}, V_{\rm ref}]$. As

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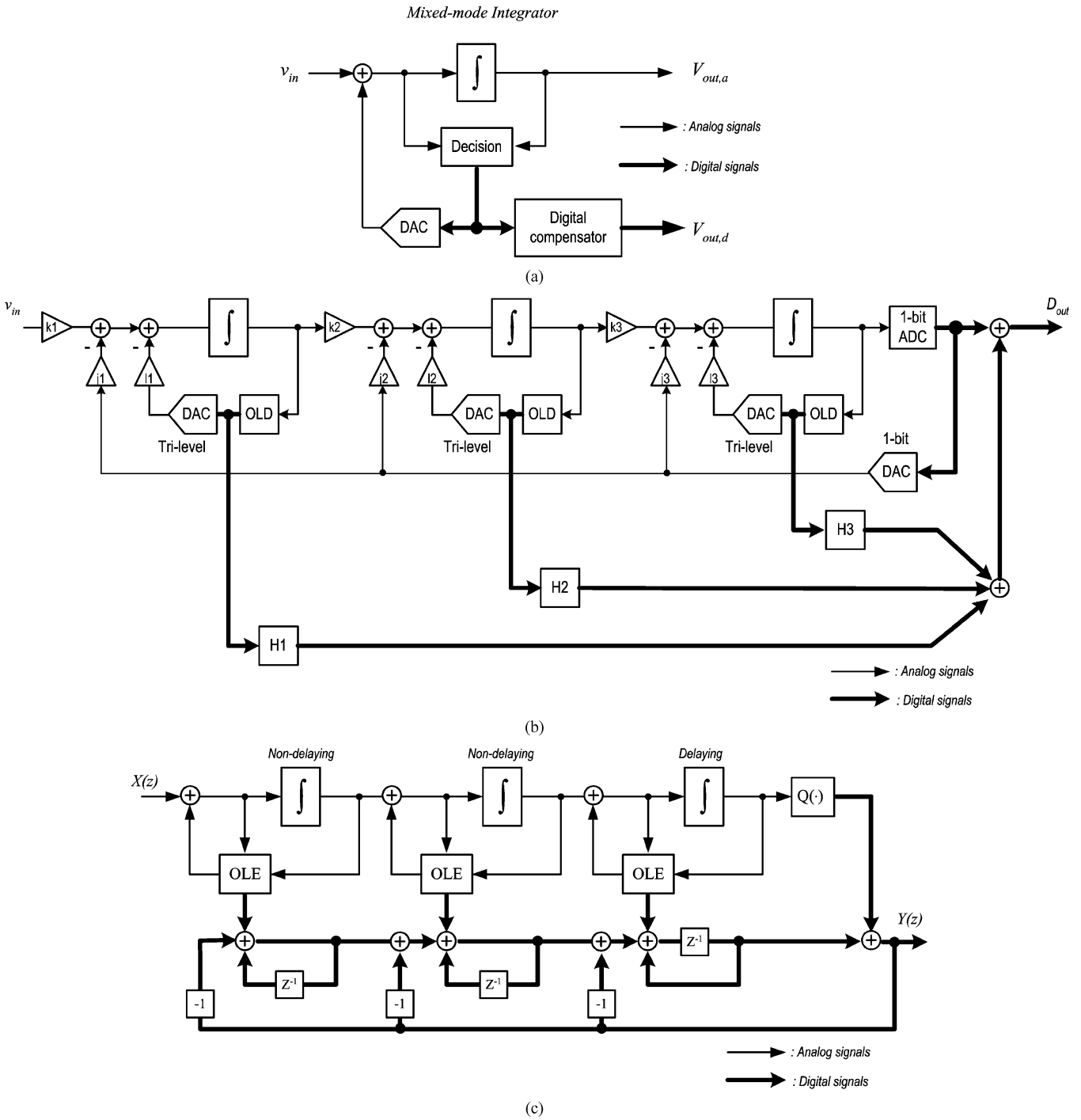

Fig. 1. (a) Integrator with a local feedback loop. (b) Single-loop third-order modulator stabilized with local feedback loops [9]. (c) Single-loop third-order modulator employing mixed-mode integrators [12].

the local feedback signal is one of $\{-2V_{\rm ref}, 0, 2V_{\rm ref}\}$, the allowed analog input range is $[-2V_{\rm ref}, 2V_{\rm ref}]$ while the integrator output is well controlled within $[-V_{\rm ref}, V_{\rm ref}]$.

Although the use of local feedbacks is an effective means to enhance the signal swing of an integrator, mismatch between analog and digital paths poses a critical problem that gives rise to increased in-band noise and tones. In order to fully exploit the benefit of the local feedbacks, the digital path should be calibrated in such a way that the transfer function of the digital path matches that of the analog path. This paper describes a third-order ΣΔ modulator that employs calibrated mixed-mode integrators. To verify the feasibility of the modulator, an experimental prototype chip was fabricated in 0.18-μm CMOS process. The outline of this paper is as follows. In Section II, the modulator architecture and a calibration technique will be described. Section III addresses circuit implementation issues and Section IV presents experimental results. Finally, a conclusion will be given in Section V.

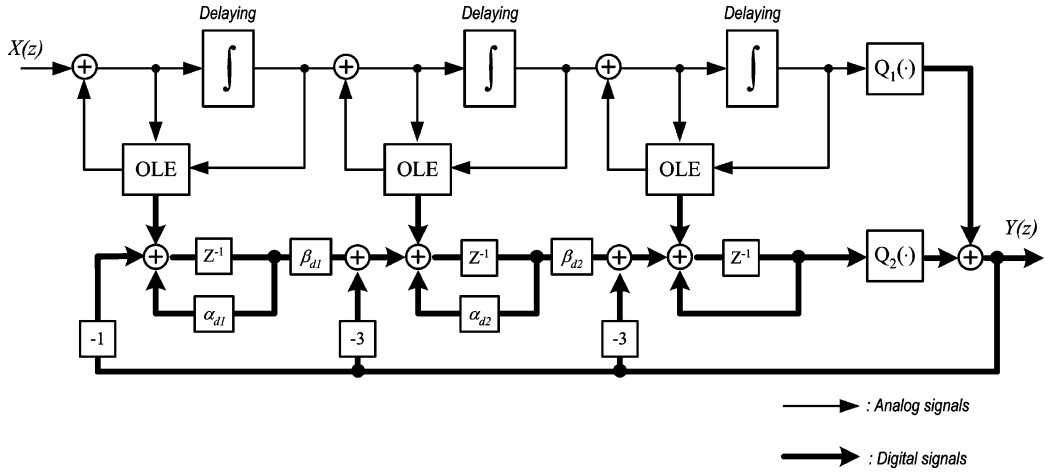

Fig. 2. Proposed third-order modulator structure.

II. Architectural Considerations

A. Modulator Structure

The modulator structure is shown in Fig. 2. The topology is basically the same as the one in Fig. 1(c), but several important modifications have been made, as described in the following.

1) All the integrators (both analog and digital) are delaying integrators, where a delay is inserted in the forward path. This delay makes pipelining of the modulator possible, thereby relaxing the speed requirement of the integrator. In order to maintain the same noise transfer function (NTF), an extra coefficient (i.e., -3) is introduced in the global feedback path, which can be done easily because it is digital.
2) The digital integrators employ additional digital coefficients (α_{d1}, β_{d1}, α_{d2}, and β_{d2}). While the ideal transfer function of a delaying integrator is given by

$$H_i(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

the transfer function of a practical analog integrator deviates from (1) as a result of imperfect analog circuits. In particular, capacitor mismatch and a finite dc gain of an amplifier alter the pole location and the gain of the integrator. The modified transfer function of the integrator can be expressed by

$$H_p(z) = \frac{\beta_a z^{-1}}{1 - \alpha_a z^{-1}}. \tag{2}$$

The digital coefficients α_{d1}, β_{d1}, α_{d2}, and β_{d2} are used to model the transfer functions of analog integrators. If not eliminated properly, mismatch would make incompletely cancelled local feedback signals leak into the modulator output. As shown in Fig. 3, where 60-dB dc gain and 0.5-% capacitor mismatch are assumed, the leakage increases in-band noises and/or tones. The leakage due to the first integrator is most serious because it is not suppressed by noise shaping [11], while the leakage from the third integrator is negligible, obviating the need for extra digital coefficients.

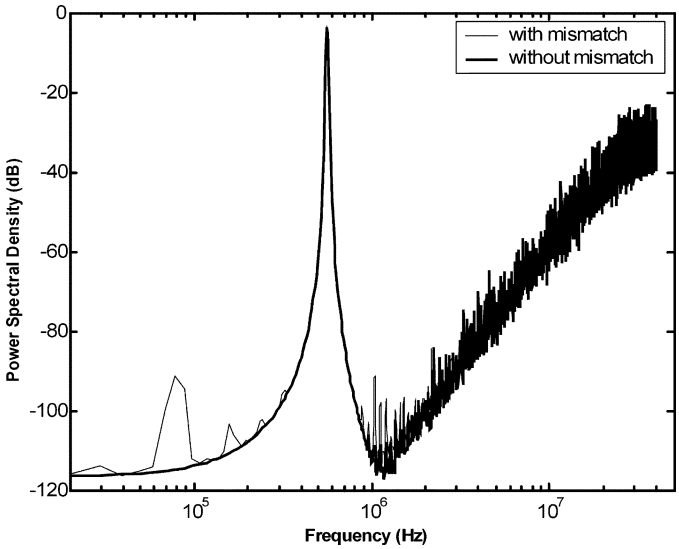

Fig. 3. Output spectra of a third-order modulator with and without mismatch.

3) An additional quantizer Q_2 is used. The digital coefficients increase the required number of bits for signals in the digital path. Q_2 truncates a few least significant bits of the input in order to decrease the bit width of the final modulator output. This helps reduce the complexity of the following decimation filter.
4) The transfer function of Q_1 is slightly modified. Fig. 4 contrasts implementations of conventional and modified 1-b quantizers. In a conventional $\Sigma\Delta$ modulator, the output of the quantizer is converted to an analog form by a DAC and fed back to analog integrators. Because the feedback level is related with the input full scale of the modulator, it should be as large as possible. In contrast, the output of Q_1 is fed only to the digital path and the input full scale is related only with the signal swing of the first mixed-mode integrator. As a result, the quantizer output level can be reduced by half as illustrated in Fig. 4(b). Since the input to the quantizer is the output of a mixed-mode integrator, the input is strictly limited within $[-V_{\rm ref}, V_{\rm ref}]$ and the maximum error due to quantization is $V_{\rm ref}/2$, which is half of the maximum error of

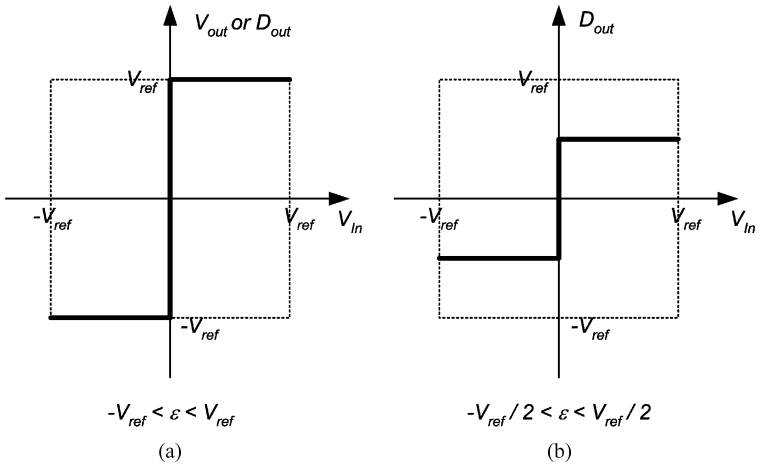

Fig. 4. Transfer functions of 1-b quantizers. (a) Conventional. (b) Modified.

a conventional quantizer. The decreased error results in 6-dB lower quantization noise power.

If all the digital coefficients are unity, the modulator in Fig. 2 realizes the third-order pure noise-differencing NTF, given by

$$\mathrm{NTF} = (1 - z^{-1})^3. \tag{3}$$

Even if the digital coefficients are not unity, the resulting NTF is approximately the same as (3) provided that the digital coefficients are close to unity. The achievable dynamic range with the noise transfer function of (3) and a 1-b quantizer is known to be

$$\mathrm{DR} = \frac{10.5}{\pi^6}\mathrm{OSR}^7, \tag{4}$$

where OSR is the oversampling ratio [3]. However, a better dynamic range is possible using the proposed modulator. The mixed-mode integrator allows us to double the full-scale input of the modulator and the modified 1-b quantizer reduces the power of quantization noise by 6 dB. In consequence, the modulator in Fig. 2 can provide a 12-dB better dynamic range. For example, the maximum achievable dynamic range of a conventional third-order modulator is 65 dB at the oversampling ratio of 16 while the proposed modulator can achieve a 77-dB dynamic range. As conventional ΣΔ modulators cannot fully achieve the dynamic range of (4) because of stability concern, the improvement could be even larger.

Because the analog path is stabilized by local feedbacks, stability of the modulator is verified if the digital path is also stable. The digital path itself is a single-loop ΣΔ modulator. Root-locus analysis indicates that the digital modulator is stable if the digital coefficients are sufficiently close to unity. The quantizer Q_2 should not pose a serious problem either because it is basically a multibit quantizer. However, extensive behavioral simulations are necessary since rigorous stability analysis is difficult.

B. Selection of Digital Coefficients

As mentioned in previous sections, the digital coefficients should be carefully chosen in such a way that they make the transfer functions of digital integrators match those of analog integrators. However, finding the optimal set of digital coefficients is not straightforward. Direct measurement of the transfer function of an analog integrator is not practical. Alternatively, selection of the coefficients can be based on the power of quantization noise. As shown in Fig. 3, the low-frequency power spectrum increases if mismatch exists between analog and digital paths. An impulse train is used as the modulator input in order to make it easy to estimate the low-frequency noise power. Since the impulse train has no spectral components below its fundamental frequency, the modulator output will contain only the in-band noise after out-of-band signals are filtered out by a decimation filter. The in-band noise power P_Q is estimated by the squared average of the decimated output minus its dc offset power, which is expressed by

$$P_Q = \frac{1}{N}\sum_{n=0}^{N-1}|y_d(n)|^2 - \left|\frac{1}{N}\sum_{n=0}^{N-1} y_d(n)\right|^2 \tag{5}$$

where $y_d(n)$ is the output of the decimation filter and N is the number of samples used.

The digital coefficients that minimize the low-frequency noise power P_Q can be obtained using a steepest descent method. The vector $\underline{g}$ of digital coefficients, $[\alpha_{d1}, \beta_{d1}, \alpha_{d2}, \beta_{d2}]^T$, are updated by means of the following recursive equation:

$$\underline{g}(n+1) = \underline{g}(n) - \mu\nabla P_Q \tag{6}$$

where μ is a small step size and ∇P_Q is the gradient of the noise power in terms of digital coefficients, which is given by

$$\nabla P_Q = \left[\begin{array}{cccc}\frac{\partial P_Q}{\partial \alpha_{d1}} & \frac{\partial P_Q}{\partial \beta_{d1}} & \frac{\partial P_Q}{\partial \alpha_{d2}} & \frac{\partial P_Q}{\partial \beta_{d2}}\end{array}\right]^T. \tag{7}$$

Calculation of ∇P_Q entails making a perturbation (δ) for each digital coefficient and evaluating the change of the noise power P_Q. The recursion relationship in (6) updates the digital coefficients in the direction that decreases the noise power most quickly and the iteration is continued until the required noise level is reached. Illustrated in Fig. 5 are the results of behavioral simulations that are performed under the conditions listed in Table I. Fig. 5(a) shows the in-band noise profile as a function of α_{d1} and β_{d1}. The steepest descent algorithm takes us to the minimum point. Examples of learning curves shown in Fig. 5(b)

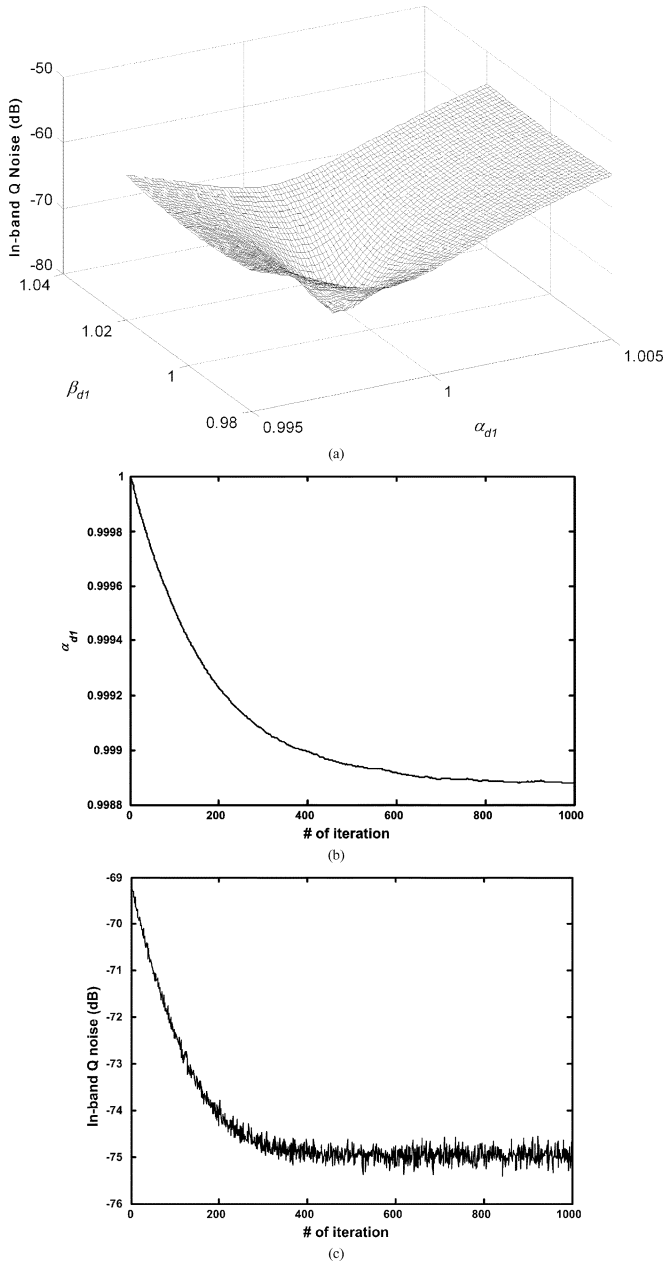

Fig. 5. Behavioral simulation results. (a) In-band Q noise profile. (b) Learning curve of α_d. (c) Learning curve of in-band Q noise.

TABLE I
CONDITIONS FOR BEHAVIORAL SIMULATION

Modulator Order	3
OSR	16
OP-AMP DC Gain	60
Capacitor mismatch	0.5 %
Sampling Frequency	3.2 MHz
Modulator Input	Impulse Train with the fundamental frequency being 0.4 MHz
Step size (μ)	4×10^{-2}
δ	10^{-4}

and (c) indicate that the optimal coefficients are reached roughly after 500 iterations have been made.

III. CIRCUIT DESIGN AND IMPLEMENTATION

The modulator is designed targeting GSM and WCDMA applications. Although the dynamic range requirements for these applications depend on the receiver architecture, typically more than 72 dB over a 200-kHz signal bandwidth and 54 dB over a 3.84-MHz signal bandwidth are required for GSM and WCDMA applications, respectively [13], [14]. The proposed modulator can meet these requirements with low OSRs, specifically 16 and 8, respectively. The corresponding clock frequencies are 3.2 MHz for GSM and 40 MHz for WCDMA.

A. Analog Integrator

The fully differential switched-capacitor integrator is depicted in Fig. 6. While integrators in conventional $\Sigma\Delta$ modulators employ gain scaling in order to limit the signal excursion, a mixed-mode integrator does not need such a scaling because its signal range is controlled by the local feedback loop. Therefore, the gain of the integrator is designed to be unity and the sampling capacitor C_s and the feedback capacitor C_f are of the same size, which is a desirable feature. The minimum size of the capacitor is dictated by kT/C noise and the total capacitance seen by the amplifier is minimized when the two capacitors have the same size.

The effects of capacitor mismatch and finite dc gains are mitigated by the use of calibrated digital integrators, thus relaxing the requirements for capacitor matching and dc gains. However, the mismatch due to nonlinearities of analog circuits such as signal-dependent gains cannot be corrected by the presented calibration technique. Consequently, analog circuits need to be carefully designed to minimize nonlinear effects. The operational amplifier, which is a fully differential cascode amplifier with a switched-capacitor common-mode feedback circuit, is designed to have a slightly low but relatively flat dc gain over the integrator output range (0.5 V). The simulated dc gain is around 60 dB and the gain drop at the edge of the output signal range is 1%. In order to reduce signal-dependent resistance, the integrator input is connected to the sampling capacitors through bootstrapped switches that are proposed in [15]. Other switches are transmission gates.

The integrator is driven by nonoverlapping two-phase clocks and their delayed versions. The timing of clocks is illustrated in Fig. 7. While ϕ_1 is on, signals are sampled on capacitors and the next output of the integrator is estimated by the OLE. During the nonoverlapping interval between ϕ_1 and ϕ_2, the OLE determines the local feedback signal based on estimation results. While ϕ_2 is on, the real next output of the integrator is evaluated and the OLE is tracking the integrator output for the use in the future.

B. Overload Estimator (OLE)

The OLE roughly calculates the next integrator output before the real value is evaluated in order to check whether the integrator will be saturated or not. If the allowed output range of the analog integrator is slightly larger than $[-V_{\rm ref}, V_{\rm ref}]$, a small error in overload estimation can be tolerated. Consequently, a simple passive network of switches and capacitors (Fig. 8) can be used for the OLE. Because the comparator output is latched

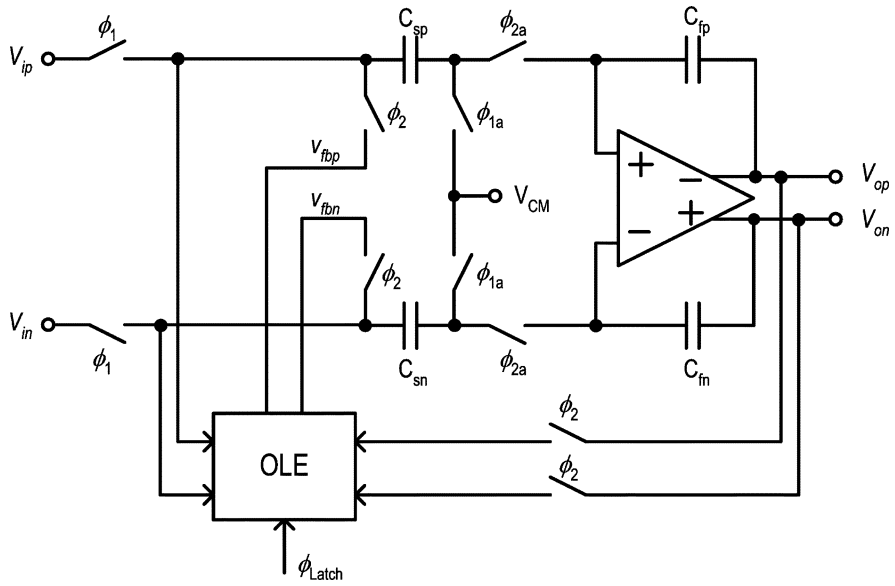

Fig. 6. Fully differential switched-capacitor integrator.

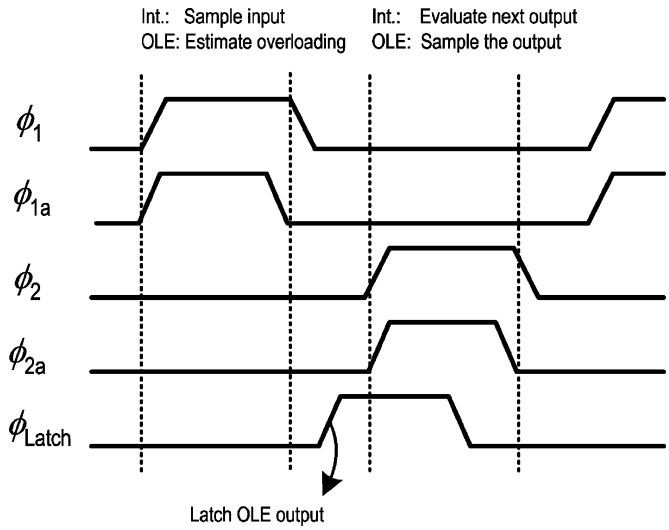

Fig. 7. Timing diagram.

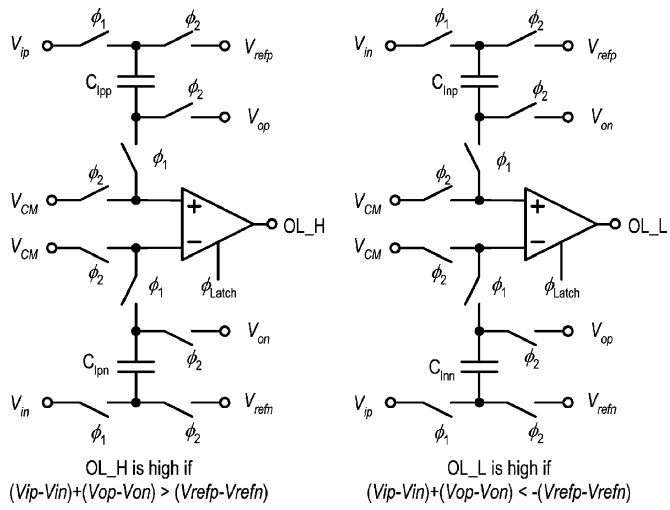

Fig. 8. Overload estimator (OLE).

during a short interval and the local feedback signal must be prepared before the rising edge of ϕ_2, comparators must be sufficiently fast. The comparator that consists of a pre-amplifier, flip-flops, and an SR latch [16] is suitable for this purpose since it exhibits fairly good speed performance. To reduce the effects of parasitic capacitors, input terminals of comparators are periodically connected to a common-mode voltage. Capacitors and switches should be as small as possible in order to minimize overheads due to the OLEs.

C. Digital Integrator

The bit widths of the digital integrator should be carefully determined so that the round-off errors do not deteriorate the performance. In addition, a sufficient number of bits should be assigned to the digital coefficients to cover the possible ranges of coefficients. Assuming the worst case dc gain of 45 dB and capacitor mismatch of 0.5%, extensive simulations have been performed, which reveal that the required bit width for α_d and β_d are 4 and 3, respectively. The register of the digital integrator needs 17 bits with some margins. Quantizer Q_2 takes only five most significant bits and truncates the other bits since the truncation error is suppressed by the feedback loop.

IV. Experimental Results

A third-order ΣΔ modulator was implemented in a 0.18-μm CMOS technology. The prototype chip was tested for GSM and WCDMA applications. In order to find the optimal digital coefficients α_d and β_d, an impulse train whose fundamental frequency is 0.4 MHz is applied to the modulator working at 3.2-MHz sampling frequency, and the OLE signals and quantizer outputs are collected. The digital path of the modulator and a decimation filter are simulated by a computer, and the collected data are processed to calculate the in-band noise. The recursive equation (6) is iterated until the optimal set of digital

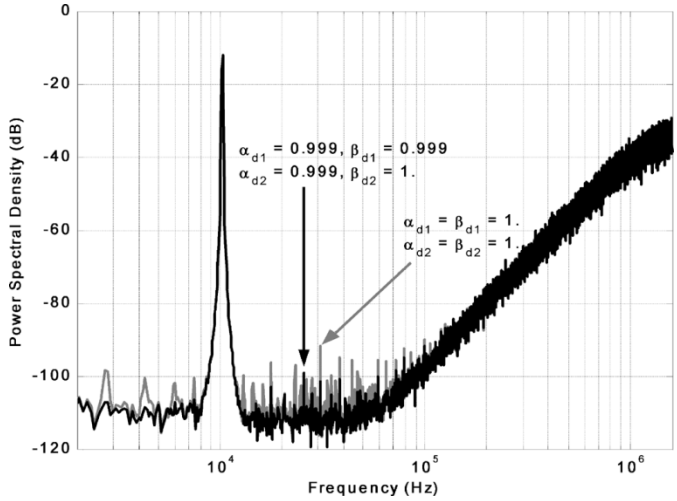

Fig. 9. Modulator output spectra of a 10-kHz sinusoidal input with 3.2-MHz sampling frequency.

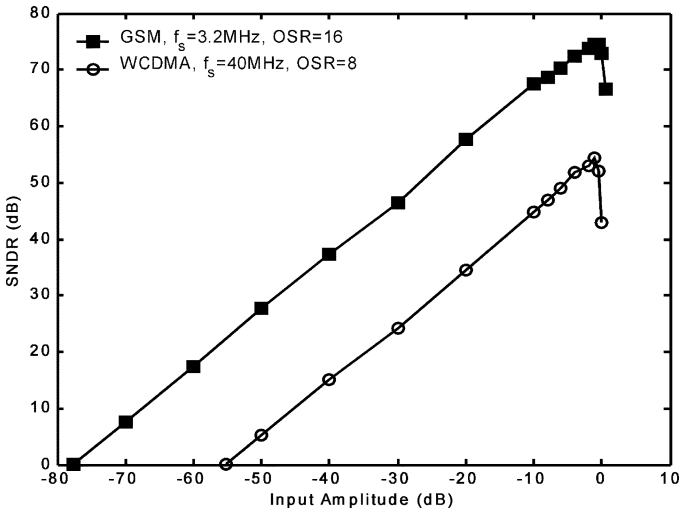

Fig. 10. SNDRs versus input amplitudes.

coefficients is obtained, and the coefficients are fitted into the finite bit width thereafter. A brute-force search in the space of α_d and β_d that have finite bit widths also results in the same set of coefficients. Fig. 9 shows the measured output spectra when a 10-kHz sinusoidal input is modulated with a 3.2-MHz sampling frequency. When proper coefficients are used, spurious tones are appreciably reduced. Fig. 10 plots the SNDRs versus the input amplitudes. The amplitude of 0 dB corresponds to the 1-Vp differential ($= 2V_{\rm ref}$). Fig. 10 also shows the case when the sampling frequency is 40 MHz and the oversampling ratio is 8. The dynamic range is 76 dB for $16 \times$ OSR and 55 dB for $8 \times$ OSR. In either case, the prototype chip dissipates 4 mW from 1.8-V supply voltages. Fig. 11 shows the chip microphotograph. The core area is 0.7 mm^2. Table II summarizes the performance. If optimal coefficients are not used, the dynamic range decreases by about 6 dB for $16 \times$ OSR; however no significant decrease is observed for $8 \times$ OSR. It is due to the fact that the dynamic range is limited mainly by the high-frequency quantization noise for low OSRs rather than mismatch-induced errors.

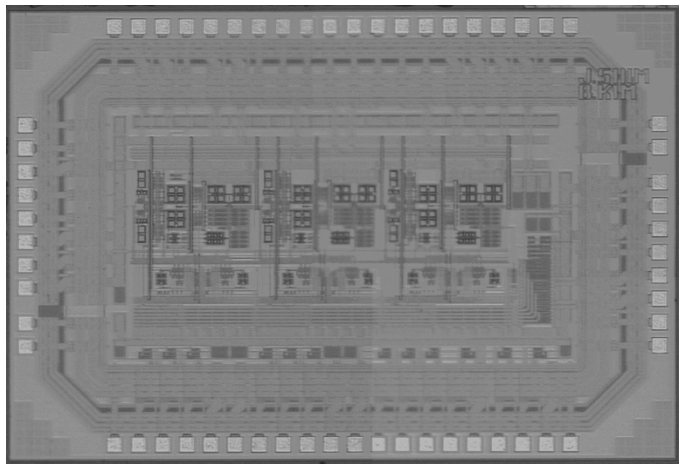

Fig. 11. Chip microphotograph.

TABLE II
PERFORMANCE SUMMARY

Application	GSM	WCDMA
Sampling Rate	3.2 MHz	40 MHz
Nyquist Rate	200 kHz	5 MHz
OSR	16	8
Dynamic Range	76 dB	55 dB
Power Consumption	4 mW	
Supply Voltage	1.8 V	
Technology	0.18-μm CMOS	

V. CONCLUSION

A single-bit third-order $\Sigma\Delta$ modulator employing mixed-mode integrators has been presented. The mixed-mode integrator offers an increased effective dynamic range with the help of the digital integrator. However, mismatch between analog and digital paths could diminish the advantage of mixed-mode integrators. The presented modulator uses digital coefficients to alleviate the mismatch effects. The experimental third-order modulator meets the dynamic range requirements of GSM and WCDMA applications with very low sampling frequencies. The modulator structure is particularly attractive for modern VLSI technologies, wherein the swing of analog signals is seriously limited while the digital circuit performance is excellent in size and power consumption.

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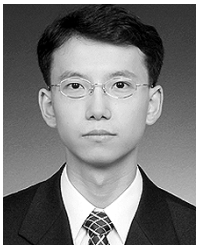

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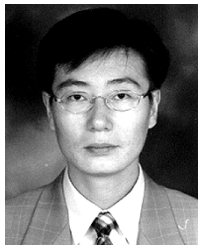

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