Hybrid $\Sigma\Delta$ Modulators With Adaptive Calibration

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***Abstract*—This paper describes an architecture for stable high-order $\Sigma\Delta$ modulation. The architecture is based on a hybrid $\Sigma\Delta$ modulator, wherein hybrid integrators replace conventional analog integrators. The hybrid integrator, which is a combination of an analog integrator and a digital integrator, offers an increased dynamic range and helps make the resulting high-order $\Sigma\Delta$ modulator stable. However, the hybrid $\Sigma\Delta$ modulator relies on precise matching of analog and digital paths. In this paper, a calibration technique to alleviate possible mismatch between analog and digital paths is proposed. The calibration adaptively adjusts the digital integrators so that their transfer functions match the transfer functions of corresponding analog integrators. Through behavioral-level simulations of fourth-order $\Sigma\Delta$ modulators, the calibration technique is verified.**

***Index Terms*—Adaptive signal processing, calibration, $\Sigma\Delta$ modulation, analog-digital conversion.**

I. Introduction

OVERSAMPLING and noise-shaping techniques have been widely employed for many high-resolution analog-to-digital converters (ADCs). Oversampling lowers the spectral power density of quantization noise, and noise shaping by $\Sigma\Delta$ modulation further reduces the in-band noise power, thereby improving the effective signal-to-quantization-noise ratio (SQNR). Since the negative feedback in a $\Sigma\Delta$ modulator effectively suppresses the quantization noise, a simple quantizer such as a 1-b quantizer can be used, obviating the need for precision analog circuitry. The simplicity of analog circuits makes high-resolution ADCs feasible with a low-cost fabrication process [1].

The main drawback of oversampling $\Sigma\Delta$ ADCs is the limited signal bandwidth. For a high resolution, the oversampling ratio should be as high as possible. However, the oversampling ratio cannot be increased arbitrarily since the maximum operation speed of analog circuits is limited by technologies. Accordingly, a high-order (>2) $\Sigma\Delta$ modulator, which aggressively attenuates the in-band quantization noise, is required to achieve a high resolution at a given oversampling ratio. When a high-order $\Sigma\Delta$ modulator is used, attention must be paid to the stability of the modulator. Internal signals of a high-order $\Sigma\Delta$ modulator may become quite large and eventually overload the quantizer, especially when a 1-b quantizer is used and the input level is near the full scale. As the output of an overloaded quantizer cannot track the large internal signals effectively, the internal signals become ever-increasing, and in the end, will be limited by the supply voltage. The limited signals in turn lead to nonlinearity generating harmonic distortion. A multibit quantizer can be used to significantly enhance the stability of a high-order $\Sigma\Delta$ modulator. The use of a multibit quantizer, however, requires a prohibitively high-linear digital-to-analog converter (DAC) because the nonlinearity of the DAC appears at the output without noise shaping.

Efforts have been made to mitigate integrator saturation and quantizer overloading [2]–[4]. Reference [2] proposed the use of overload detectors (OLDs) and local feedback. If an OLD detects saturation of the integrators, a local feedback signal is added to the input summing junction of the integrator, thus preventing saturation of the integrator. Digital filters cancel the local feedback signals. The architecture was employed to stabilize a third-order modulator in [3]. Recently, a hybrid $\Sigma\Delta$ modulator architecture using mixed-mode or hybrid integrators has been proposed [4]. In essence, the structure of a hybrid modulator is equivalent to that of [3]. However, a hybrid $\Sigma\Delta$ modulator uses overload estimators (OLEs) instead of OLDs, and the cancellation filter for local feedback signals are simpler. In addition, the hybrid structure is more suitable for using a multibit quantizer. In either architecture, the performance relies on exact matching of analog and digital paths, necessitating appropriate calibration. In this paper, an adaptive calibration technique for hybrid $\Sigma\Delta$ modulators is presented to improve the matching of analog and digital paths.

This paper is organized as follows. Section II briefly explains the architecture of the hybrid $\Sigma\Delta$ modulator and addresses its advantages. In Section III, the mismatch effect is analyzed, and a calibration technique is proposed to remove the mismatch. Section IV presents design examples of adaptively calibrated fourth-order hybrid modulators along with simulation results. Finally, conclusion is drawn in Section V.

II. Hybrid Modulators

Fig. 1 illustrates the block diagram of a $\Sigma\Delta$ modulator. If the terms b_n are the binomial coefficients, it realizes the Lth-order noise-differencing modulation and the transfer function of the modulator is given by

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^L E_Q(z) \tag{1}$$

where $E_Q(z)$ is the additive noise due to quantization. If a 1-b quantizer is used, the dynamic range of the noise-differencing modulator with the oversampling ratio (OSR) is [5]

$$\mathrm{DR} = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)\mathrm{OSR}^{2L+1}. \tag{2}$$

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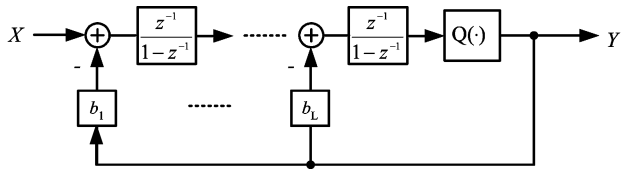

Fig. 1. L^{th}-order $\Sigma\Delta$ modulator.

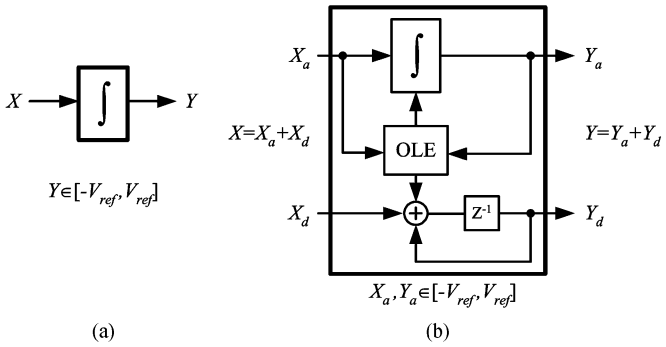

Fig. 2. Block diagrams of (a) analog integrator and (b) hybrid integrator.

Unfortunately, high-order $(L > 2)$ noise-differencing modulators are unstable when a 1-b quantizer is used. Therefore, different noise transfer functions other than noise-differencing must be used for high-order modulators, but this generally results in a smaller dynamic range than that in (2). Even for first- and second-order modulators, which are stable, the direct implementation of Fig. 1 requires too large integrator output swing, and therefore appropriate signal scaling must be used to prevent integrator saturation or quantizer overloading. A hybrid $\Sigma\Delta$ modulator in the following provides a good solution for implementation of stable high-order noise-differencing modulators.

Fig. 2 shows block diagrams of a conventional integrator and a hybrid integrator. A mixed-mode or hybrid integrator [4], [6] is a combination of an analog integrator and a digital integrator. As shown in Fig. 2(b), the input and output of the hybrid integrator are composed of an analog component and a digital component. The analog component is bounded within $[-V_{\text{ref}}, V_{\text{ref}}]$, and V_{ref} is limited by the power supply voltage. On the other hand, the digital component may take an arbitrarily large value if a sufficient number of bits are used in the digital integrator. Even if the input analog component is bounded within $[-V_{\text{ref}}, V_{\text{ref}}]$, the analog integrator output may exceed the allowed range depending on the previous output value. In reality, the analog output will be limited or saturated, causing nonlinearity. To prevent saturation of the analog integrator, the hybrid integrator employs OLEs similar to the OLDs of [3]. An OLE pre-evaluates the analog output. If the result is not in the range of $[-V_{\text{ref}}, V_{\text{ref}}]$, $2V_{\text{ref}}$ is added to or subtracted from the analog component, and the opposite operation is applied to the digital component instead. The pre-evaluation calls for only a slight increase in settling-time requirements because overload estimation does not have to be accurate; a small error in overload estimation is tolerable if the estimation error is smaller than the margin between V_{ref} and $V_{\max}$, wherein $V_{\max}$ is the physically-allowed maximum of the analog integrator output. If the bit-width of the digital integrator is sufficiently wide, the hybrid integrator is free from saturation. Consequently, the dynamic range of the hybrid integrator can be easily controlled as desired. This is an attractive feature for modern very large-scale integration (VLSI) technologies with lowered supply voltages.

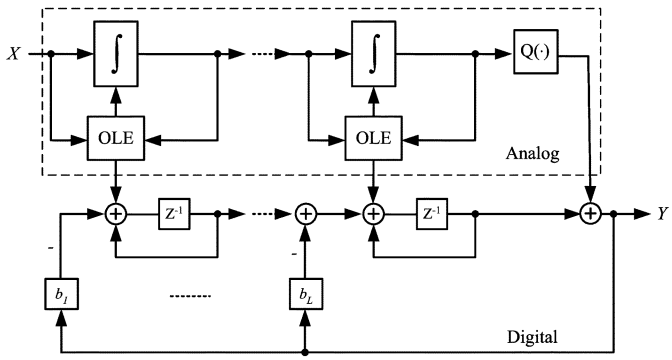

Fig. 3.Hybrid $\Sigma\Delta$ modulator.

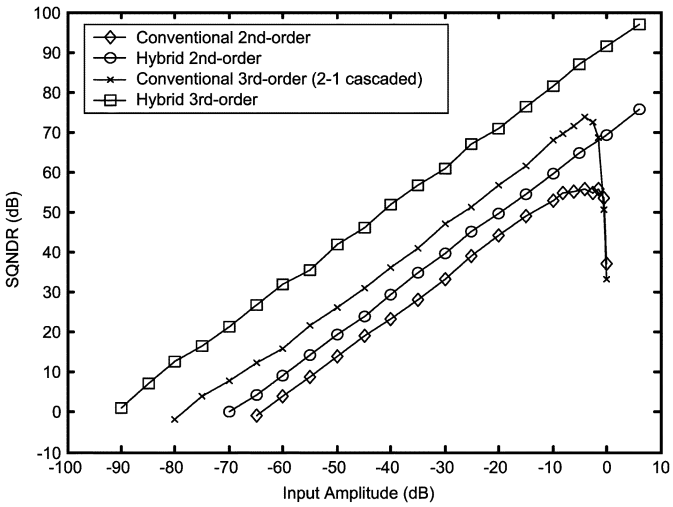

Fig. 4. SQNDRs versus input amplitudes of $\Sigma\Delta$ modulators $(\text{OSR} = 32)$.

Fig. 3 shows the block diagram of a hybrid $\Sigma\Delta$ modulator. The structure is basically the same as a conventional single-stage $\Sigma\Delta$ modulator except that hybrid integrators replace analog integrators. The analog integrators are stabilized by local feedbacks formed by OLEs, and the outputs are bounded in $[-V_{\text{ref}}, V_{\text{ref}}]$. As a result, quantizer overloading does not occur. Furthermore, no global feedback signal exists in the analog part because global feedback signals are all fed to the digital path. Consequently, the analog part is stable. As for the digital part, it is basically a linear stable system when the terms b_n are the binomial coefficients; the digital part does not contain any nonlinear component, and the transfer function has no pole. Because both the analog and the digital parts are stable, the hybrid $\Sigma\Delta$ modulator is also stable. Hybrid $\Sigma\Delta$ modulators have another useful feature. Since no global analog feedback exists, a high-linear DAC is not required even if a multibit quantizer is used in the analog path.

Fig. 4 shows the performance of four $\Sigma\Delta$ modulators. Each modulator employs a 1-b quantizer, and the oversampling ratio is 32. The input level of V_{ref} corresponds to 0 dB. The conventional second-order modulator is based on the architecture presented in [7] wherein each integrator has a gain of

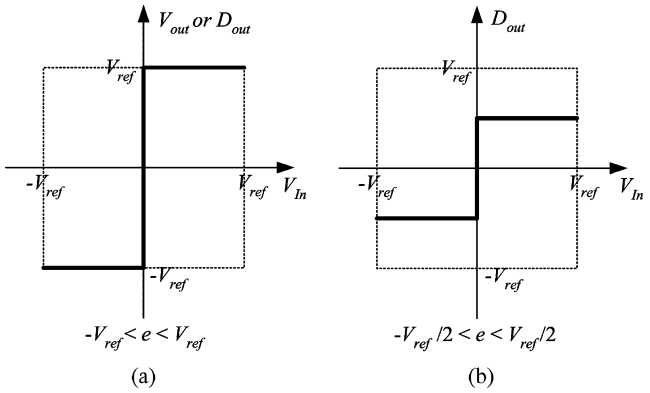

Fig. 5. 1-b quantizers of (a) conventional modulators and (b) hybrid modulators.

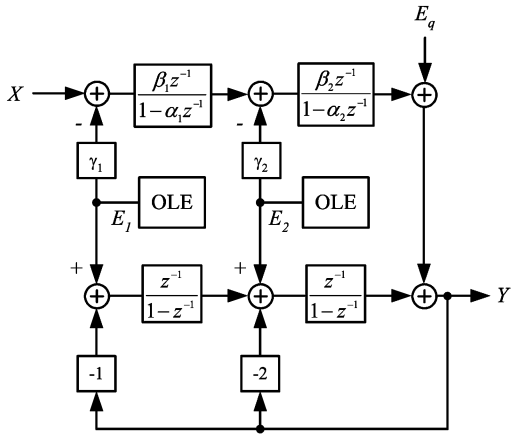

Fig. 6. Second-order hybrid ΣΔ modulator with analog circuit imperfections.

$1/2$. The conventional third-order modulator is a 2-1 cascaded architecture with the inter-stage coupling gain of $1/4$ [8]. It is observed that the hybrid modulators exhibit better dynamic ranges than the conventional modulators. Signal-to-quantization-noise-plus-distortion ratios (SQNDRs) of hybrid modulators do not degrade even for 6-dB input amplitude because the OLE of the hybrid integrator keeps the analog output within $[-V_{\rm ref}, V_{\rm ref}]$ as long as the input amplitude is smaller than $2V_{\rm ref}$. By contrast, SQNDRs of the conventional modulators begin to degrade at the input level of about -3 dB. In addition, the SQNDR of the hybrid second-order modulator is about 6 dB larger than that of the conventional second-order modulator at the same input amplitude. It is due to different implementation of the 1-b quantizer. Fig. 5 contrasts two implementations of the 1-b quantizer. Since the allowed full-scale input of a conventional modulator is closely related to the output levels of the quantizer or the feedback DAC, the quantizer output should be as large as possible. For a hybrid modulator, however, the full-scale input is determined solely by the output swing of the analog integrator regardless of the quantizer output level. If the quantizer output level is reduced by half as shown in Fig. 5(b), the quantization noise power is lowered by 6 dB, hence the 6-dB increase in SQNDR of the hybrid modulator. For the 2-1 cascaded modulator, the inter-stage gain of $1/4$ causes additional 12-dB reduction in SQNDR compared with the hybrid third-order modulator. An increased inter-stage gain improves the peak SQNDR, but degradation of the SQNDR will begin at lower input amplitudes. In general, the dynamic range of a hybrid ΣΔ modulator using a 1-b quantizer is about 12 dB larger than that in (2), which is calculated based on the assumption that the full-scale input power is

$$P_{S,c} = \frac{1}{2}V_{\rm ref}^2 \tag{3}$$

and the quantization noise power is

$$P_{Q,c} = \frac{1}{12}(2V_{\rm ref})^2 = \frac{1}{3}V_{\rm ref}^2 \tag{4}$$

while the powers of the full-scale input and the quantization noise of a hybrid modulator are

$$P_{S,h} = \frac{1}{2}(2V_{\rm ref})^2 = 2V_{\rm ref}^2 \tag{5}$$

and

$$P_{Q,h} = \frac{1}{12}(V_{\rm ref})^2 \tag{6}$$

respectively.

Hybrid ΣΔ modulators consist of analog and digital integrators. As with cascaded ΣΔ modulators, hybrid ΣΔ modulators are very sensitive to the mismatch between analog and digital paths. Unfortunately, the mismatch due to imperfection of analog circuits is inevitable. In Section III, the effect of the mismatch is identified, and a calibration technique for coping with the mismatch is presented.

III. Adaptive Calibration

A. Mismatch Between Analog and Digital Paths

While digital integrators perfectly implement the ideal transfer function

$$H_d(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{7}$$

transfer functions of analog integrators deviate from (7) because of the imperfections of analog circuits, which include capacitor mismatch, finite amplifier gains, and incomplete or nonlinear settling [7]. In particular, capacitor mismatch and finite amplifier gains affect the pole location and the gain of the integrator, as expressed by

$$H_a(z) = \frac{\beta z^{-1}}{1 - \alpha z^{-1}}. \tag{8}$$

The output of a hybrid integrator is then given by

$$\begin{aligned} Y(z) &= H_a(z)(X_a(z) - E(z)) + H_d(z)(X_d(z) + E(z)) \\ &= H_a(z)X_a(z) + H_d(z)X_d(z) + (H_d(z) - H_a(z))E(z) \end{aligned} \tag{9}$$

where $X_a(z)$ and $X_d(z)$ are the analog and digital input, respectively, and $E(z)$ is the OLE output. Different transfer functions for $X_a(z)$ and $X_d(z)$ together with incompletely cancelled $E(z)$ cause nonlinear behavior of hybrid integrators, eventually leading to performance degradation of ΣΔ modulators. The following relation is easily obtained from Fig. 6, which shows a

second-order hybrid $\Sigma\Delta$ modulator with nonideal analog integrators:

$$\begin{aligned} Y(z) &= \left\{(X(z)-\gamma_1 E_1(z))\,\frac{\beta_1 z^{-1}}{1-\alpha_1 z^{-1}} - \gamma_2 E_2(z)\right\}\frac{\beta_2 z^{-1}}{1-\alpha_2 z^{-1}} \\ &\quad + \left\{(E_1(z)-Y(z))\frac{z^{-1}}{1-z^{-1}} + E_2(z) - 2Y(z)\right\} \\ &\quad \times \frac{z^{-1}}{1-z^{-1}} + E_q(z). \end{aligned} \tag{10}$$

Rearranging (10) leads to

$$\begin{aligned} Y(z) &= \beta_1\beta_2 z^{-2}\frac{(1-z^{-1})^2}{(1-\alpha_1 z^{-1})(1-\alpha_2 z^{-1})}X(z) \\ &\quad + (1-z^{-1})^2 E_q(z) \\ &\quad + z^{-2}\left\{1 - \frac{\beta_1\beta_2\gamma_1(1-z^{-1})^2}{(1-\alpha_1 z^{-1})(1-\alpha_2 z^{-1})}\right\}E_1(z) \\ &\quad + z^{-1}(1-z^{-1})\left\{1 - \frac{\beta_2\gamma_2(1-z^{-1})}{(1-\alpha_2 z^{-1})}\right\}E_2(z). \end{aligned} \tag{11}$$

For a hybrid $\Sigma\Delta$ modulator of order L, (11) can be rewritten as

$$\begin{aligned} Y(z) &= X(z)(1-z^{-1})^L \prod_{k=1}^{L} H_{a,k}(z) + (1-z^{-1})^L E_q(z) \\ &\quad + \sum_{k=1}^{L}(1-z^{-1})^{k-1} \\ &\quad \times \left\{z^{-(L+1-k)} - (1-z^{-1})^{L+1-k}\gamma_\kappa \prod_{n=k}^{L} H_{a,n}(z)\right\}E_k(z) \\ &\approx z^{-L}X(z) + (1-z^{-1})^L E_q(z) \\ &\quad + \sum_{k=1}^{L}(1-z^{-1})^{k-1} \\ &\quad \times \left\{z^{-(L+1-k)} - (1-z^{-1})^{L+1-k}\gamma_\kappa \prod_{n=k}^{L} H_{a,n}(z)\right\}E_k(z) \\ &= \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E_q(z) + \sum_{k=1}^{L} F_k(z)E_k(z). \end{aligned} \tag{12}$$

Although (11) and (12) are based on inaccurate linear models that do not take into account correlations between $X(z), E_q(z)$, and $E_k(z)$, they provide insight on the effect of mismatch. Firstly, the signal transfer function and the noise transfer function are almost ideal, but incompletely cancelled OLE signals $E_k(z)$ leak to the output, thus decreasing the SQNR. Secondly, the effect of $E_1(z)$ is dominant because all the transfer functions for $E_k(z)$ except for $k = 1$ have the noise-shaping term, $(1 - z^{-1})$. Since the transfer function for $E_1(z)$ is of low-pass type, the mismatch effect is most serious at low frequencies. Fig. 7 shows output spectra of a fourth-order hybrid $\Sigma\Delta$ modulator with and without mismatch. When mismatch exists, the noise level and spurs increase at low frequencies. As the mismatch is detrimental, calibration is necessary for hybrid $\Sigma\Delta$ modulators.

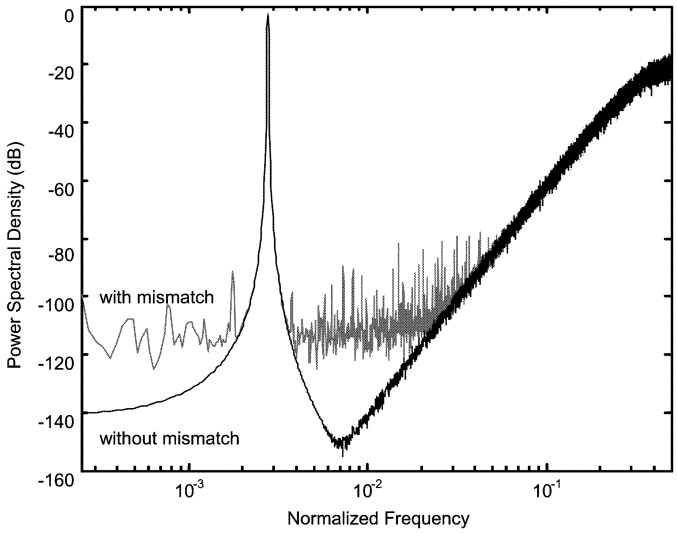

Fig. 7. Output spectra of a fourth-order hybrid $\Sigma\Delta$ modulator with and without mismatch.

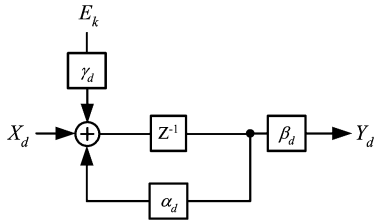

Fig. 8. Digital integrator with gain coefficients.

B. Calibration

The goal of calibration is to make analog and digital integrators have the same transfer function. While analog integrators are difficult to calibrate, digital integrators can be easily controlled by introducing gain coefficients, as shown in Fig. 8. For calibration, the digital coefficients that match the coefficients of analog integrators must be found. The resulting transfer function of the hybrid integrator may be different from the ideal transfer function (7), but it would have little effect on overall performance. When the mismatch is eliminated, the hybrid $\Sigma\Delta$ modulator is equivalent to a conventional single-stage $\Sigma\Delta$ modulator, except that it is free from integrator saturation and quantizer overloading. A conventional single-stage $\Sigma\Delta$ modulator is known to be rather tolerant of analog imperfections [7], [9].

As indicated in Fig. 7, quantization noise power increases at low frequencies when the mismatch exists. At high frequencies, the noise power is the same whether the mismatch exists or not. A calibration technique using this property is possible, where the digital coefficients are adaptively updated until low-frequency noise power is minimized. Because the calibration technique is based on an estimation of noise power, the estimation must be done accurately and easily. Since useful information is available only at low frequencies, the estimation of noise power is performed on data from which the high-frequency components have been removed. In a $\Sigma\Delta$ ADC, the decimation filter removes the out-of-band signal and decimates the result; consequently, the output of the decimation filter contains only the in-band signal, and its data rate is low. Therefore,

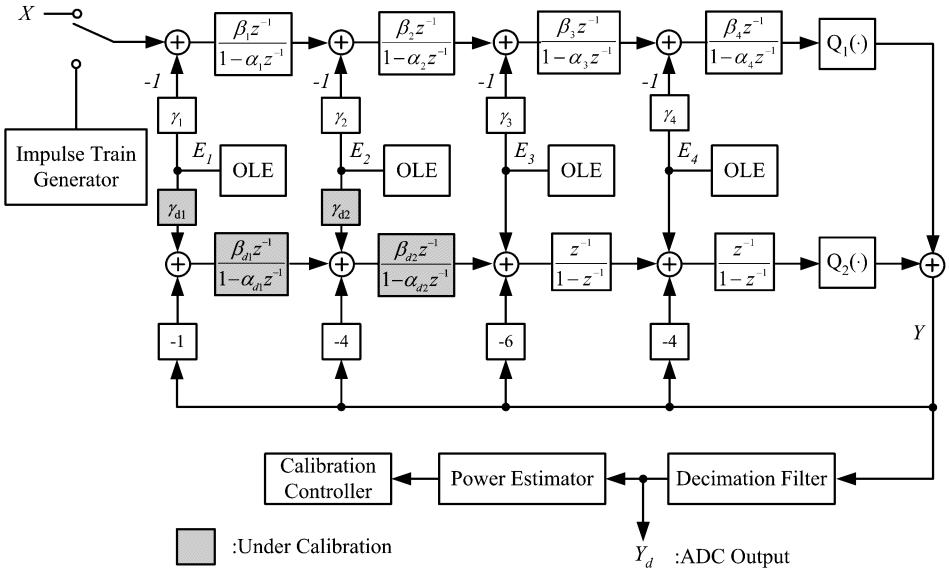

Fig. 9. Fourth-order ΣΔ ADC with the proposed calibration technique.

the decimation filter output is useful for the estimation of noise power.

If input signals exist in a low-frequency band, distinguishing their power from noise power is difficult. To ease the power estimation, no signal should be in the band of interest. However, this does not mean that input signals should not exist at all. A signal with sufficient power must be supplied to the hybrid ΣΔ modulator to invoke the OLEs. A particularly useful input is an impulse train whose fundamental frequency is on an out-of-band frequency. On-chip generation of an impulse train is relatively straightforward for switched-capacitor implementation; a voltage reference of a sufficient magnitude is periodically connected to the modulator input using a switch controlled by a counter.

The in-band quantization noise power P_Q is estimated by

$$P_Q = \frac{1}{N}\sum_{n=0}^{N-1}|y_d(n)|^2 - \left|\frac{1}{N}\sum_{n=0}^{N-1} y_d(n)\right|^2 \tag{13}$$

using N samples of the decimation filter output $y_d(n)$, which contains only the quantization noise and leaked OLE outputs. The digital coefficients are adaptively updated so that the noise power is minimized using the steepest descent method based on the following recursive relationship:

$$\underline{g}(n+1) = \underline{g}(n) - \mu\nabla P_Q \tag{14}$$

where $\underline{g}$ is a vector of the digital coefficients $(\alpha_d, \beta_d, \gamma_d)$ to be updated, μ is the step size, and ∇P_Q is the gradient of P_Q in terms of the digital coefficients. The step size should be sufficiently small for convergence. Calculating the gradient involves disturbing each digital coefficient by a small amount (δ) and measuring the change in the noise power. When the dimension of $\underline{g}$ is large, the gradient calculation is time-consuming and requires a large memory. Therefore, restricting the number of coefficients to be adjusted at the cost of a slight degradation in performance could be a good tradeoff.

TABLE I
SUMMARY OF SIMULATION RESULTS

Quantizer	Calibration				Peak SQNDR (dB)
	1st	2nd	3rd	4th	
1-b Quantizer	O	O	O	O	91.9
	O	O	X	X	**91.5**
	O	X	X	X	73.4
	X	X	X	X	65.7
3-b Quantizer	O	O	O	O	103.9
	O	O	X	X	**102.1**
	O	X	X	X	75.5
	X	X	X	X	68.2

IV. DESIGN EXAMPLES AND SIMULATION RESULTS

A. Design Examples and Simulation Results

In this section, application of the proposed calibration technique to fourth-order hybrid ΣΔ modulators is considered. Fig. 9 illustrates the block diagram of an adaptively calibrated fourth-order hybrid ΣΔ ADC. During calibration, the input switch is connected to the input pattern generator and an impulse train is supplied to the ADC. Based on the information from the noise power estimator, which implements (13), the adaptation controller calibrates only the first two digital integrators to simplify the digital part of the modulator. The effects of un-calibrated integrators, however, are negligible (see Table I).

When calibration is applied to a digital integrator, the output of the integrator is a wide-bit digital signal, and hardware complexity of the digital path increases. The quantizer Q_2 in Fig. 9 truncates some least significant bits of the digital path output, thus simplifying the digital path of the modulator and the decimation filter at the cost of a slight increase in quantization noise power.

Behavioral-level simulations were performed to verify the calibration technique. The quantizer Q_1 is a 1-b quantizer. Amplifier gains of analog integrators are modeled to be about 60 dB. Capacitor ratios are assumed to follow the Gaussian distribution

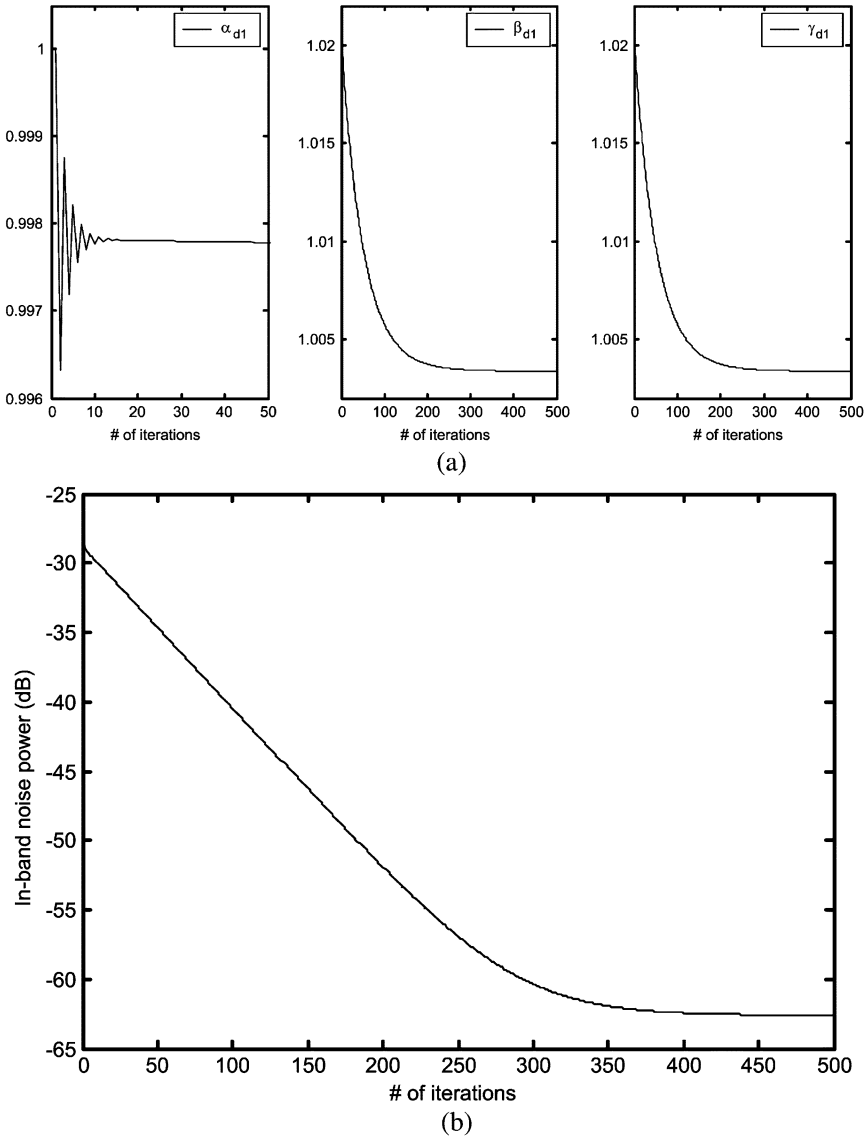

Fig. 10. Learning curve example for (a) digital gain coefficients and (b) the in-band quantization noise.

with a mean 1 and a standard deviation of 1%. The oversampling ratio is 16. The step size μ is $2 \cdot 10^{-2}$, and the small disturbance δ is 10^{-4}. When calibration was applied, the digital coefficients converged after about 400 iterations, as shown Fig. 10. Unfortunately, the calibration process may converge to local optimal points. However, convergence to local optima can be easily detected by examining the in-band quantization noise power. If the in-band noise power is greater than a specific value, the calibration process starts again from a different initial point. Since α_1 and α_2 are always smaller than 1, the initial values of α_{d1} and α_{d2} are fixed to 1. However, $\beta_i, \gamma_i (\mathrm{i} = 1, 2)$ may be greater than 1 and initial values of their corresponding digital coefficients are chosen from $\{1.02, 0.98\}$. Extensive simulations indicate that hybrid modulators can be properly calibrated using one of 16 initial-point sets.

As shown in Fig. 11, calibrating only the first two integrators drastically improves the dynamic range of the modulator. SQNDRs of un-calibrated or partially-calibrated modulators are much smaller especially when the input signal power is greater than about -50 dB, where the OLE of the first hybrid integrator starts working. The digital coefficients of un-calibrated integrators are all set to unity.

Accommodating a multibit quantizer for hybrid $\Sigma\Delta$ modulators is easy because a high-linear multibit DAC is not required. Fig. 12 shows the simulation results when a 3-b quantizer was used for Q_1. When properly calibrated, the improvement of SQNDR was about 12 dB, which is accounted for by the additional two bits of the quantizer Q_1. If the modulator is not calibrated, it cannot benefit from the multibit quantizer because the harmonic tones are dominant. Table I summarizes the simulation results.

Although finite dc gains and capacitor mismatch modify the transfer function of an analog integrator, they do not affect the linearity of the integrator and their effects can be mitigated by the proposed calibration scheme. Incomplete settling due to the limited bandwidth of an amplifier can be also fixed as long as the settling process is linear. However, other nonidealities such as input-dependent gains and slew-rate limitation cause nonlinear

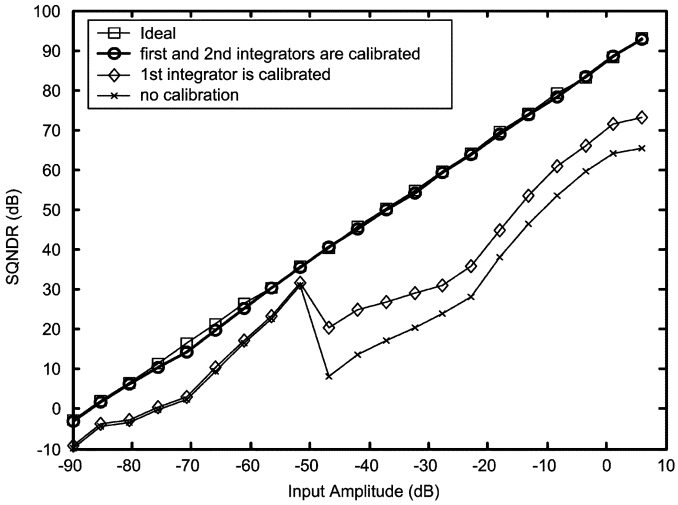

Fig. 11. SQNRs for different input levels of fourth-order hybrid ΣΔ modulators with a 1-b quantizer.

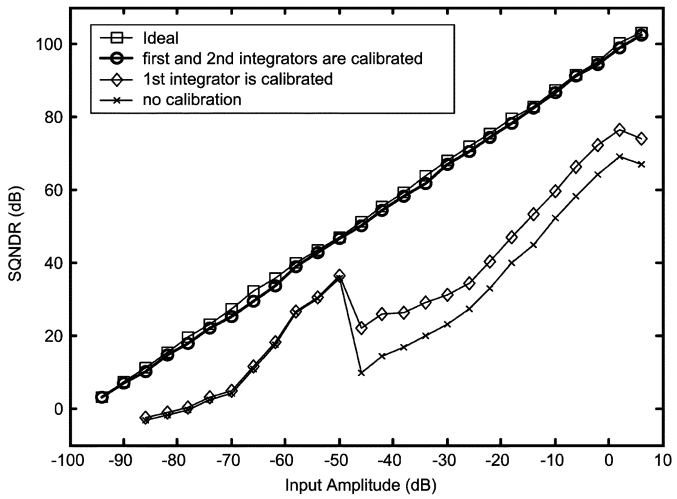

Fig. 12. SQNRs for different input levels of fourth-order hybrid ΣΔ modulators with a 3-b quantizer.

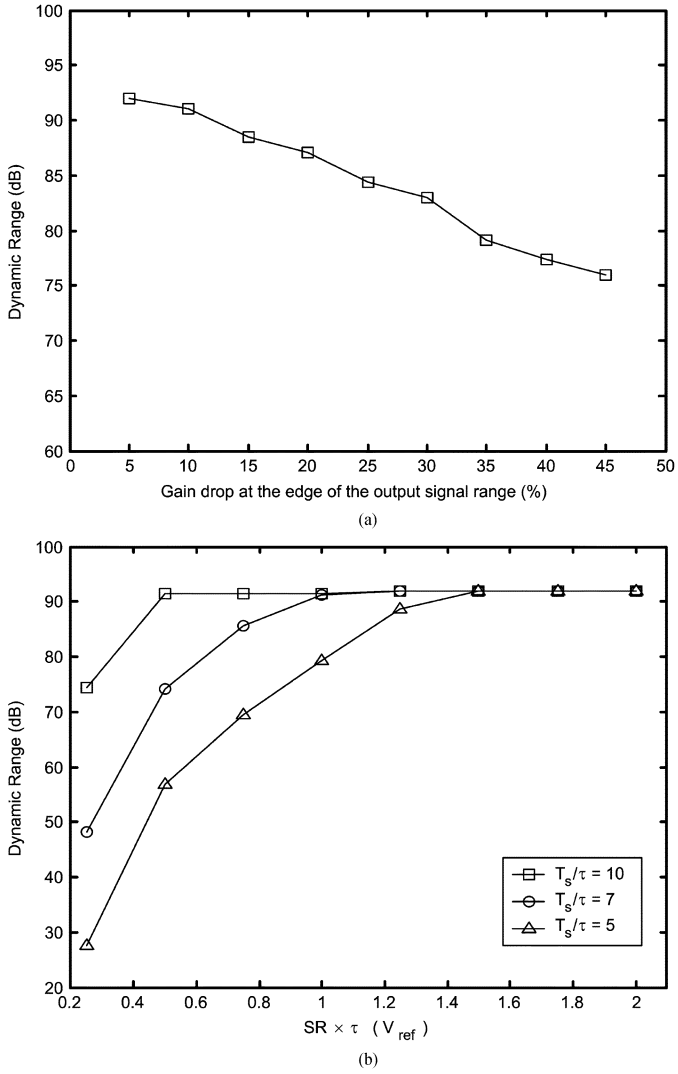

Fig. 13. Influence of integrator nonlinearity on the fourth-order hybrid ΣΔ modulator with a 1-b quantizer: (a) input-dependent gain and (b) slew-rate limited settling.

behavior of analog integrators and cannot be fixed by the proposed calibration. Fig. 13 shows the influence of nonlinearity on the dynamic range of the hybrid fourth-order ΣΔ modulator. In Fig. 13(a), the amplifier gain is nominally 60 dB and its input dependency is modeled by Taylor series. Simulation results indicate that about 10% reduction in gain at the edge of the output range is tolerable. Nonlinear settling is particularly troublesome for hybrid modulators because slew-rate limitation may occur frequently when OLEs work actively. The first-order model of settling characteristics in [10] was used to investigate the effects of slew-rate limitation, and the simulation results are summarized in Fig. 13(b). If $\mathrm{SR} \times \tau$ is greater than $2V_{\mathrm{ref}}$, where *SR* is the integrator slew rate and τ is the integrator settling time constant, settling process is always linear. However, using large $\mathrm{SR} \times \tau$ is not always possible; in particular, $\mathrm{SR} \times \tau$ is closely related to the over-drive voltage of integrator input transistors in CMOS switched-capacitor implementation. Fig. 13(b) indicates that the sampling period T_s should be long enough compared with the time constant to minimize the effect of slew-rate limitation.

B. Discussion

In Section II, it is shown that the hybrid ΣΔ modulator is stable because both the analog and digital parts are stable systems. When calibration is applied to the hybrid modulator, however, the stability is not readily verified. The analog path is still stable, but the digital coefficients α_d, β_d, and γ_d may jeopardize the stability of the digital path. Furthermore, the quantizer Q_2 in Fig. 9 makes the digital part a nonlinear system, thus making stability analysis difficult. Fortunately, since the quantizer Q_2 is a multibit quantizer, the linear model that is commonly used in analysis of ΣΔ modulators is useful. Using the linear model, the pole locations of the modulator can be traced for various values of digital coefficients to check the stability. However, the stability must be finally checked by extensive simulations. Simulation results indicate that the fourth-order hybrid modulator in Fig. 9 is stable if digital coefficients are sufficiently close to unity.

The main drawback of the proposed modulator structure is the hardware complexity for digital integrators and adaptation

control circuits. For the hybrid fourth-order modulator depicted in Fig. 9, four real multipliers are required to implement $\alpha_{d1}, \alpha_{d2}, \beta_{d1}$, and β_{d2} (for γ_{d1} and γ_{d2} can be realized using only adders), and the adders are all multibit adders to maintain the precision of the multiplications. Since the digital block operates at the oversampling cock, the digital circuits must be fast enough. Therefore, the digital path could be a bottleneck for wide-band applications. The speed requirements for the power estimator and the calibration controller are relaxed because they process the decimated output, but they would require considerable digital hardware as well. As VLSI technologies advance, however, the speed and size of digital paths will be improved while analog paths face more stringent constraints such as reduced power supply voltages. Therefore, the proposed hybrid $\Sigma\Delta$ modulator is an attractive architecture for modern VLSI systems.

Cascaded structures have been popular choices for stable high-order $\Sigma\Delta$ modulation [11]. In cascaded $\Sigma\Delta$ modulators, digital noise-cancellation filters cancel out the quantization noises from the intermediate stages. Since noise cancellation relies on matching of analog and digital paths, cascaded structures are also sensitive to imperfections of analog circuits. To mitigate the mismatch effect, digital correction techniques based on adaptive control over noise-canceling filters have been proposed [12]–[15]. The adaptively calibrated hybrid $\Sigma\Delta$ modulator presented in this paper is similar to the cascaded $\Sigma\Delta$ modulator with digital correction; overload estimators are analogous to intermediate-stage quantizers of the cascaded modulator, and digital integrators correspond to noise cancellation filters. Both structures apply adaptive calibration to digital paths to correct the imperfections of analog circuitry. However, the calibrated hybrid modulator is different from the digitally corrected cascaded $\Sigma\Delta$ modulator in the following standpoints. Firstly, the digital part of a hybrid modulator has a global feedback path while the cascaded modulator does not. The output of the calibrated hybrid modulator is wide-bit digital signals but some least significant bits of the output can be truncated (using Q_2 in Fig. 9) without any serious degradation of SQNDR because the truncation error is suppressed by the digital feedback loop. This is particularly useful because it simplifies the decimation filter. Secondly, the SQNDR of the calibrated hybrid modulator does not degrade at high input signal levels as long as nonlinearity of the analog path is not serious. On the other hand, since the sub-modulators of the cascaded modulator can use only a fraction of the feedback reference level $V_{\rm ref}$, the SQNDR of the cascaded modulator decreases at high input signal levels. Finally, the quantizer output of the hybrid modulator is not fed to the analog path. Therefore, using multibit quantizer is relatively easier.

V. Conclusion

In this paper, an adaptively calibrated hybrid $\Sigma\Delta$ modulator has been presented as a possible architecture for high-order noise shaping. This architecture applies an adaptive calibration to the hybrid $\Sigma\Delta$ modulator to remove or reduce the mismatch between analog and digital paths which is shown to increase the in-band noise of the modulator output. Using a steepest descent method, the calibration scheme adaptively adjusts the coefficients of the digital integrators so that the in-band noise and distortion are minimized. Extensive simulations of the fourth-order hybrid modulator indicate that the proposed architecture can be used to implement high-order noise shaping without any stability problem. However, simulations also indicate that for high-performance $\Sigma\Delta$ modulators, the analog integrator still must be carefully designed so that nonlinearity of the analog integrator does not impair the modulator performance because the proposed calibration scheme cannot fix the nonlinearity. The proposed architecture is particularly attractive for modern VLSI technologies, which impose significant constraints on the dynamic range of the analog circuits but dramatically improve the power dissipation and size of digital circuits.

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