function of the applied gate voltage. When the devices are saturated, the current is increasing with the square of $V_{DS}$.

The smallest device, however, has a linear range of close to 2.5 V in strong inversion with less than 1% relative error. As pointed out in [9], short-channel effects degrade the device to a linear function of $V_{GS}$, which may be explored for extended linear behaviour also when the device is saturated.

Owing to bulk capacitance ($C_g$) the circuit is sensitive to common-mode changes. A common-mode feedback circuit setting the $V_{fg}$ voltage may be included, compensating for these errors in the micro-power biasing scheme of Fig. 2. Other errors, such as mismatch, have not been accounted for in the simulations, but should not severely affect the operation of the circuit except for 'normal' spread in the equivalent resistive value.

It is possible to estimate the equivalent resistance against applied gate voltage. Fig. 4 shows these results and an equivalent resistance may be tuned from kΩ to GΩ (six orders of magnitude).

*Conclusions:* We have presented a novel single transistor circuit for implementation of resistive equivalents in microelectronics. Capacitive feedback of drain-source voltage and short channel effects are explored extending the linear range to 2.5 V with <1% relative error. The resistance may be tuned over six orders of magnitude.


*2 June 2003*
*Electronics Letters Online No: 20030820*
*DOI: 10.1049/el:20030820*

T.S. Lande and E. Olsen (*Department of Informatics, University of Oslo, Norway*)

C. Toumazou (*EE Dept., Imperial College, London, United Kingdom*)

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## Quadrature direct digital frequency synthesis using fine-grain angle rotation technique

Sung-Won Lee and In-Cheol Park

An area- and power-efficient quadrature direct digital frequency synthesis technique called fine-grain angle rotation is presented. To reduce the large bitwidth requirement of the angle rotation, multiple start points are introduced and the angle rotation is applied to the remaining small angle. A prototype chip occupies 0.16 mm$^2$ in 0.25 μm 1P5M CMOS technology and consumes 90 mW at 400 MHz clock frequency, which is a significantly improved performance compared to previous state-of-the-art chips.

*Introduction:* The direct digital frequency synthesiser (DDFS) plays a crucial role in agile frequency and spread-spectrum communications systems due to its fast frequency switching capability, continuous phase, fine frequency resolution, and good spectral purity. Most DDFSs are composed of a phase accumulator and a sine/cosine generator [1]. ROM-based lookup schemes are widely used in the sine/cosine generation. As the ROM takes considerable area, several compression techniques were proposed [2]. For the applications requiring high spurious free dynamic range (SFDR) such as tunable digital bandpass filters and mixers for digital receivers, angle rotation schemes based on scalable modular architectures [3, 4] have an advantage in that the size increases linearly. However, the angle rotation techniques usually require larger internal bit resolution than the output resolution to prevent the accumulation of round-off errors. The large internal resolution leads to large area and causes more power consumption. An interpolative angle rotation technique [5] was proposed to reduce the resolution requirement. The technique achieves a small reduction of the internal bit resolution but fails to reduce the area and power consumption. In this Letter we describe an efficient direct digital frequency synthesis technique called fine-grain angle rotation that reduces internal bit resolution and achieves less area and power consumption.

*Fine-grain angle rotation:* For a given phase $\theta$, $\cos\theta$ and $\sin\theta$ are computed by applying two steps: a table lookup for the coarse phase and an angle rotation for the fine phase remained. As shown in Fig. 1, $\theta$ is decomposed into three parts. The first 3-bit part represents the $\pi/4$ symmetry exploited to cover any phase in $(0, 2\pi)$. The second $N$-bit part is the coarse phase to be used to lookup two tables that contain $2^N$ cosine/sine entries with a bit resolution $L$. The lookup values are start points of the fine angle rotation of the remaining $K$-bit part. Each table entry stores an accurate value of $\cos(\pi/4 \cdot (n \cdot 2^{-N} + 2^{-N-K-1}))$ or $\sin(\pi/4 \cdot (n \cdot 2^{-N} + 2^{-N-K-1}))$, where $n$ is an integer, $0 \le n < 2^N$ and $2^{-N-K-1}$ is introduced to compensate the phase gap caused by the $\pi/4$ symmetry calculation. While the table size increases exponentially according to the input bit width, it increases linearly according to its output size. Therefore, if we control $N$ to be small, the two tables can be implemented without the compression technique [2]. The usage of tables is different from previous angle rotation schemes [4] that reduce a number of initial stages by storing the intermediate values resulting from the initial stages into tables.

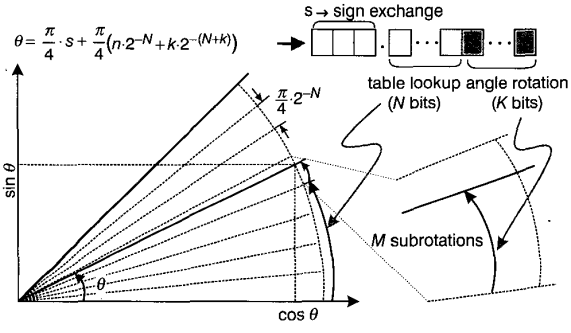


**Fig. 1** *Basic concept of fine-grain angle rotation*

Next, an angle rotation is applied to rotate the given start point by $\theta_k = \pi/4 \cdot (k \cdot 2^{-(N+K)})$, where $k$ is an integer, $0 \le k < 2^K$. The CORDIC algorithm [3] can compute the angle rotation by decomposing $\theta_k = \sum_i \sigma_i \cdot \text{atan}(2^{-i})$, where $\sigma_i \in \{-1, 1\}$. As the CORDIC algorithm uses a successive approximation to decide $\sigma_i$, the redundant carry-save arithmetic is hardly exploited and additional comparing logic is necessary, impeding a high speed and low-power implementation. Fortunately, the table lookup let $\theta_k$ to have $N$ leading-zeros as $\pi/4 < 1$. In this case, the rotation can be computed at a time by determining $N$ and $K$ such that the $\sigma_i$ prediction scheme [6] becomes valid. Let us consider $\theta_k$ with $N$ leading zeros

$$\theta_k = 0.00\cdots0x_{N+1}x_{N+2}\cdots x_{2N+2}\cdots x_{3N+3}x_{3N+4}\cdots \quad (1)$$

As $\text{atan}(2^{-i}) = 2^{-i} - 2^{-3i}/3 + \cdots$, the prediction of $\sigma_i$'s is possible by setting $\sigma_i = 1$ for $i = N+1$, and $\sigma_i = 2(x_{i-1} - 1/2)$ for $N+1 < i \le$

$3N+4$. Therefore, if $K<2N$, the angle rotation by $\theta_k$ can be calculated using $\sigma_i$'s determined directly from the prediction.

Let $X_{n,N}$ and $Y_{n,N}$ be the lookup values corresponding to the cosine and sine of the coarse phase, respectively. Then the sequence of subrotations are expressed as

$$X_{n,i+1} = X_{n,i} - \sigma_{i+1}2^{-i-1}Y_{n,i} \quad \text{and} \quad Y_{n,i+1} = Y_{n,i} + \sigma_{i+1}2^{-i-1}X_{n,i} \tag{2}$$

where $N \le i \le 3N+4$. The values having completed $M$ subrotations, $X_{n,N+M}$ and $Y_{n,N+M}$ can be approximated for $N \ge L/3$ as follows

$$\begin{aligned} X_{n,N+M} &\cong X_{n,N} - Y_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} - 2^{-N-1}\cdot X_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} \\ Y_{n,N+M} &\cong Y_{n,N} + X_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} - 2^{-N-1}\cdot Y_{n,N}\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} \end{aligned} \tag{3}$$

Compared to the approximation in [4], the third term is newly introduced to make the approximation valid for small $N$, and to improve the precision and the spurious performance as well. Replacing $\sigma_i$ with $2x_{i-1}-1$ for $i>N+1$, we have

$$\sum_{i=N+1}^{N+M}\sigma_i 2^{-i} = 2^{-N-1} + \sum_{i=N+2}^{N+M}(2x_{i-1}-1)2^{-i} \cong \sum_{i=N+1}^{N+M-1}x_i 2^{-i} = \theta_k \tag{4}$$

which means $\theta_k$ can be used in the multiplication directly. The scaling factor [3, 4] is not considered in the above calculation because its effect on the final output is negligible. The simulation result shows that a DDFS designed with $N=7$, $K=9$, $M=10$, and $L=16$ achieves 15.0 bits precision and 114 dBc SFDR, while a DDFS using 16-stage angle rotation with $L=16$ has 11.5 bits precision and 91.5 dBc SFDR. To achieve the same performance as the proposed one, the 16-stage angle rotation should have $L=20$.

*Implementation:* The block diagram of the prototype DDFS chip is shown in Fig. 2. A 32-bit phase accumulator is partitioned into two 16-bit carry select adder sections, and its 32-bit output is truncated into 19 bits. The three most significant bits are used to control the direction of input phase and sign/exchange at the output. The 16-bit phase is decomposed into upper 7 bits ($N$) and lower 9 bits ($K$). The internal bit resolution $L$ is set to 16 bits to achieve SFDR exceeding 114 dBc. The sine/cosine tables have 128 ($2^N$) entries of 16-bit values and are optimally synthesised in combinational random logic from a PLA style description. As the 9-bit phase is a normalised value, a radian converter implemented with a simple constant multiplier is employed to obtain a corresponding radian value. The upper 9-bit values of the cosine/sine tables and the 10-bit ($M$) output of the radian converter are multiplied using two $9 \times 10$ unsigned multipliers that employ a Wallace-tree structure and two-stage pipeline. After the final addition/subtraction, 16-bit sine/cosine values are produced.

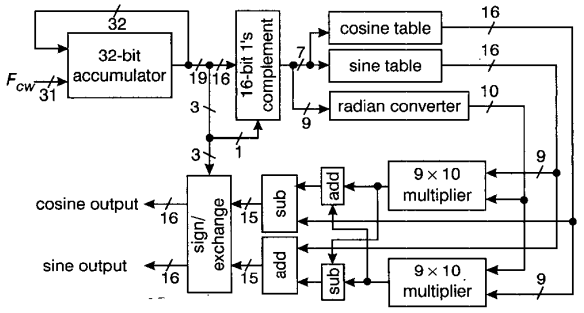


**Fig. 2** *Block diagram of prototype DDFS chip*

*Result:* The prototype chip was designed in a 0.25 µm 1P5M CMOS technology. Fig. 3 shows a layout of the chip, the active core of which occupies 0.16 mm$^2$. The maximum operating clock frequency is 400 MHz and simulated power consumption is 90 mW with 2.5 V power supply. The frequency tuning resolution is 0.09 Hz. Table 1 summarises the performance of the proposed DDFS and previous DDFS chips designed for high resolution and spurious performance.

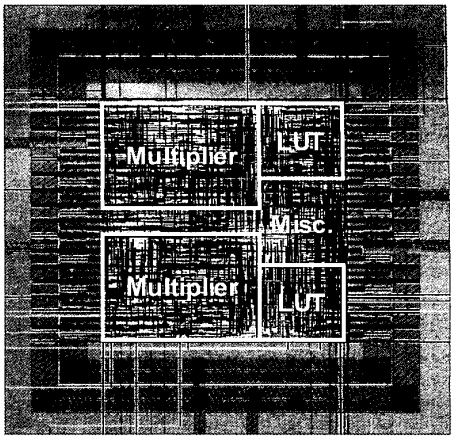


**Fig. 3** *Layout of prototype DDFS chip*

**Table 1:** Performance comparison with previous DDFS chips

| | Nicholas [2] | Madisetti [4] | Song [5] | This work |
|---|---|---|---|---|
| Process | 1.25 µm (5 V) | 1.0 µm (5 V) | 0.35 µm (3.5 V) | 0.25 µm (2.5 V) |
| Type | Cosine only | Quadrature | Quadrature | Quadrature |
| Internal resolution | 11 bits | 22 bits | 18 bits | 16 bits |
| Output | 12 bits | 16 bits | 16 bits | 16 bits |
| SFDR | 90.3 dBc | 100 dBc | 96 dBc | 114 dBc |
| Max clock | 150 MHz | 100 MHz | 150 MHz | 400 MHz |
| Power | 950 mW at 100 MHz | 1400 mW at 100 MHz | 670 mW at 150 MHz | 90 mW at 400 MHz |
| | 9.5 mW/MHz | 14 mW/MHz | 4.5 mW/MHz | 0.23 mW/MHz |
| Area | 24.5 mm$^2$ | 12 mm$^2$ | 3.4 mm$^2$ | 0.16 mm$^2$ |

*Conclusion:* We have presented a quadrature direct digital frequency synthesis based on fine-grain angle rotation. The proposed technique is effective in achieving large reduction of the internal bit resolution of the angle rotation. From the prototype chip design, we found that the technique results in significantly compact design and low-power consumption even compared to state-of-the-art DDFS chips.

*Acknowledgments:* This work was supported by the IDEC and the MICROS Center.


*12 June 2003*
*Electronics Letters Online No: 20030795*
*DOI: 10.1049/el:20030795*

Sung-Won Lee and In-Cheol Park (*Department of Electrical Engineering and Computer Science, KAIST, 373-1 Guseong-Dong Yuseong-Gu, Daejeon 305-701, Republic of Korea*)

E-mail: icpark@ee.kaist.ac.kr

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## Detection of solvents using distributed fibre optic sensor

A. MacLean, C. Moran, W. Johnstone, B. Culshaw, D. Marsh and P. Parker

A fibre optic sensor that is capable of distributed detection of liquid solvents is presented. Sensor interrogation using optical time domain reflectometry (OTDR) provides the capability of locating solvent spills to a precision of ±2 m over a total sensor length that may extend to 20 km.

*Introduction:* In this Letter an optical fibre sensor capable of making fully distributed measurements of a wide range of solvents is identified. Microbending principles have been used to develop the sensor such that it responds on contact with liquid solvents, typically within 30 seconds of exposure. The sensor incorporates a swelling polymer and optical fibre components that are readily available in the optical communications industry. A conventional optical time domain reflectometry (OTDR) technique is utilised for sensor interrogation and location of multiple spill events over a range of 20 km. The sensor uses a low-power laser source to perform the sensing function and due to its optical nature is intrinsically safe. The operational characteristics of the sensor and the underlying technology utilised in its operation are described. The swelling characteristics of the polymer material in a range of solvents and experimental test results of prototype sensors are presented.

*Sensor design:* The sensor structure consists of a central glass reinforced plastic strength member 0.9 mm in diameter coated with a 100 μm thick silicone polymer (Dow Corning Silastic rubber). A graded index multimode optical fibre (Plasma 62.5/125 graded index PCVD fibre) is held against it by helically wrapping a 100 μm diameter Kevlar™ thread along the sensor length as shown in Fig. 1. The silicone polymer swells on contact with the solvents without dissolving; the extent being dependent on the activating solvent and the particular silicone polymer used. The swelling induced by the presence of the solvent causes the optical fibre to be forced against the Kevlar thread, thus inducing periodic lateral deformation. The optical fibre then experiences localised periodic microbending, causing light propagating in the fibre to be coupled between the highest guided modes and nearest cladding modes where it is attenuated. The period of the deformation determines the degree of attenuation that occurs. It was found by Fields [1] that maximum mode coupling occurs when the deformation is equal to a specific periodic spacing Λ, given by

$$\Lambda = \frac{2\pi a}{\sqrt{(2\Delta)}} \quad (1)$$

where $a$ is the radius of the fibre core and Δ is the maximum relative difference between refractive indices of the core and cladding of the fibre. It was observed by Fields [1] and later by Deimeer [2] that a multiple of this period could be used to induce mode coupling due to the equal propagation constants of adjacent modes. For the multimode fibre used in the sensor, Λ was calculated at approximately 1 mm, thus it is possible to apply the Kevlar wrap with a pitch of 2, 3, and 4 mm to cause mode coupling to occur during sensor activation.

The sensor is interrogated using standard optical time domain reflectometry (OTDR) principles. OTDR operates by sending a short pulse of light down the optical fibre and monitoring the intensity of the light that is scattered back along the fibre. The OTDR trace displays the single pass loss as a function of distance down the fibre, appearing as a line with negative gradient for a fibre with uniform loss. Positions where the loss exceeds the inherent loss of the fibre appear as sections with increased gradient, as shown in Fig. 2.

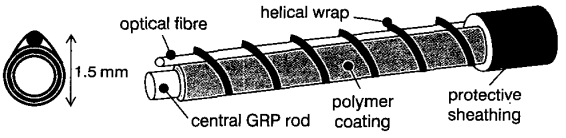


**Fig. 1** *Sensor construction*

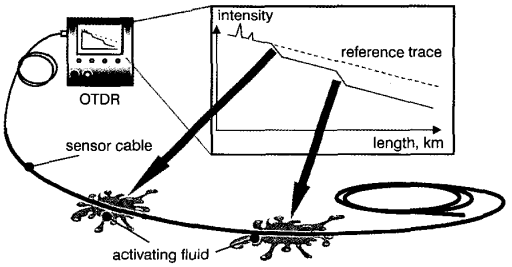


**Fig. 2** *Schematic diagram of sensor operation*

*Material analysis:* To determine solvents suitable for detection by the sensor, the silicone used was subjected to a series of tests to estimate the swelling characteristics. It was assumed that the swelling experienced by the silicone could be inferred from the degree of solvent uptake. Small thin samples were weighed when dry and then placed either directly into the solvent or suspended above it in a sealed container. The silicone samples were then removed at regular intervals over a one-hour period to be weighed. It was observed from the experiment that the maximum solvent uptake was achieved typically within 30 seconds when the samples were placed directly into the solvents. Maximum solvent uptake was achieved typically within 1 hour for samples suspended in the solvent vapour. Fig. 3 demonstrates the significant difference in solvent uptake for silicone samples placed directly into the solvent and suspended in the vapour. From previous sensor work using swelling hydrogels [3] it was observed that a weight increase of more than 65% was sufficient to cause a swelling capable of inducing a force on the optical fibre in the sensor. Using this criterion, the experimental results suggested that silicone was suitable for detection of all the solvents tested in liquid form, with the exception of acetone. The volatile vapours of chloroform, petroleum ether, cyclohexane, toluene and dichloromethane induced a weight increase that should also be readily detected since the fluid uptake values exceed the 65% threshold. Neither methyl-ethyl-ketone nor acetone in vapour form induced a solvent uptake value that would be detected using silicone in the current sensor design.

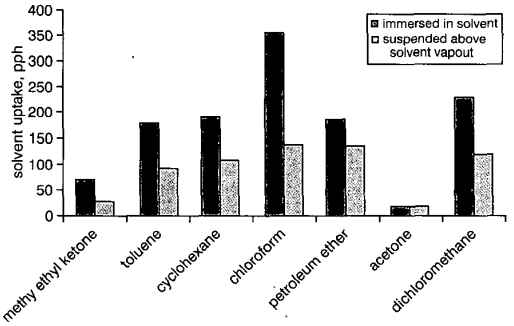


**Fig. 3** *Swelling of silicone suspended above and immersed in solvents*

*Prototype sensor testing:* Using the materials knowledge from the above tests, several prototype sensors were manufactured with the assistance of Pinacl Communications using the silicone described in the preceding Section and a 62.5/125 graded index multimode fibre. The optical fibre was coated with Hytrel™, a chemically resistant material incorporated to prevent damage to the outer acrylate layer. The central GRP rod was coated with the silicone to a thickness of 100 μm by drawing it through a silicone solution and curing it at an elevated temperature in excess of 150°C. The Kevlar was wrapped